MITSUBISHI
PROGRAMMABLE CONTROLLER
MELSEC-K

Instruction Manual

Data Link System

3(NA)-64457-A

MITSUBISHI ELECTRIC

Mitsubishi Programmable Controller

Programmable Controller MELSEC-K

Data Link System Operation Manual

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1. Outline

The data link system for the MELSEC-K series is a system which executes series or parallel data communication between several programmable controllers or I/O units and serves to reduce the wiring work expenses for long distance input and output and to permit expansion of the total number of I/O points and dispersed control.
Control information exchange with personal computers and other computers also is possible.

System 1: Parallel data link system between K2CPUs

This system is used for parallel operation between 2 or 3 K2CPUs close to each other, and it is used when the number of I/O points exceeds 512 points or when the number of program steps exceeds 4 K steps.

System 2: Remote I/O system between K2CPU and K0 units

This system is used for series I/O data communication between a K2CPU and up to max. seven K0 units as remote I/O units of the K2CPU, and it is used for reduction of the wiring work expenses for long distance input and output.

System 3: Remote I/O system with a K2CPU and I/O units for K1, K2

While the system 2 uses K0 units as remote I/O units for the K2CPU, this system uses I/O units for K1, K2, installed on a basic base for K1, as remote I/O units. Up to 7 units can be connected. This system also is used to reduce the wiring work expenses for long distance input and output. A wide variety of I/O units can be used.

System 4: Dispersed control system with K2 and K0

This system uses a K2 as master programmable controller and up to seven K0 units as local programmable controllers for series data communication between the master programmable controller and the local programmable controllers, and it is used for expansion of the total number of I/O points and for dispersed control.

Total number of I/O points: Max. 1,120
I/O points of the master programmable controller: Max. 224
I/O points of each local programmable controller: Max. 128

System 5: Dispersed control system with K2 and K2

While the system 4 uses K0 as local programmable controllers, this system uses K2 as local programmable controllers. (K2 use for master and local programmable controllers.) For system 4, the max. total number of I/O points is 1,120 points, and the max. number of I/O points for each local programmable controller is 128 points, and this system is used when the above point numbers are exceeded.

Total number of I/O points: Max. 1,792
I/O points of the master programmable controller: Max. 224
I/O points of each local programmable controller: Max. 224

System 6: Computer link system

This system is used for data communication between K2 and personal computers or other computers, and it serves for monitoring of the operation status of the K2 programmable controller by the computer, data collection, etc.

Notes:

1) Combination of the above systems for composition of systems with a still higher hierarchy also is possible, but in this case, consultations with our company should be made during the sales talks.

2) K2CPU-S3 must be used for all K2CPUs to be used for this data link system.
The K2CPU-S3 is the superior type of the standard K2CPU, the K2CPU-S1, and the K2CPU-S2, and it includes all of their functions.

3) The number of I/O points mentioned for the systems 4 and 5 can be expanded still further. For details, refer to item 5.7.

4) Mixed use of the systems 1 to 5 is possible. See item 7.

2. Data link control unit

The outline of the various units prepared for data link systems will be explained.

2.1. K2CPU-S3

This is the CPU for control of the data link system, and it includes the functions of the standard K2CPU, the K2CPU-S1, and the K2CPU-S2.
As already stated above, only the type K2CPU-S3 can be used as K2CPU for the data link system.

2.2. Parallel data link unit (KJ61)

- o This unit is used to compose the parallel data link system 1 between K2CPUs.
- o The configuration is the same as for the I/O unit for K1 and K2.
- o 16 I/O points.

2.3. Series data link control unit (KJ71)

- o This is the series data communication control unit on the K2 side for the systems 2 to 6.
- o Built-in microprocessor (8085) and 2 kbyte RAM.
- o 2 data link adapters (KJ81, KJ82) can be installed.
  However, one KJ81 or KJ82 is installed for use with the systems 2 to 6.
- o An installation socket for a data communication control ROM (L2ROM, L3ROM, L4ROM) is built in. (MBM2732A-35: 2 units can be installed.)
- o 32 I/O points.

2.4. Series data link control unit (KJ72)

- o Remote control unit for system 3.
- o Installation in the K1CPU position of the K1 base unit (K12B, K15B, K18B).
- o Built-in microprocessor (8085) and 2 kbyte RAM.
- o 1 data link adapter (KJ81) can be installed.

- o A data communication control ROM (L5ROM) is installed.

2.5. High-speed link adapter (KJ81)

- o Adapter for data transmission and reception at high speed (250 KBPS).
- o Used installed in KJ71, KJ72, or K0 unit.
- o Built-in series transmission and modem function.

2.6. RS-232C adapter (KJ82)

- o Adapter for EIA standard RS-232C interface.
- o Used installed on KJ71 for system 6.

3. RAM and ROM for data link control

For the systems 2 to 6, the following ROMs with stored control programs for data communication and RAMs for temporary data storage are available.

(1) L1ROM: Control ROM on the K0 side for system 2 and system 4.

(2) L1RAM: RAM on the K0 side for system 2 and system 4.

(3) L2ROM: ROM for KJ71 on the master side for the systems 2 to 5.

(4) L3ROM: ROM for KJ71 on the local side for system 5.

(5) L4ROM: ROM for KJ71 for system 6 (computer link).

(6) L5ROM: ROM on the KJ72 side for system 3.

At the time of ordering, specify the following part and type names. Shipping will be executed in sets.

System	Part name	Type name	Set contents
2, 4, K0 side	K0 data link set	K0DLS	KJ81, L1RAM, K1ROM
2 to 5, master side	Data link master set	KJ71L2	KJ71, KJ81, L2ROM
5, local side	K2 local set	KJ71L3	KJ71, KJ81, L3ROM
6	Computer link set	KJ71L4	KJ71, KJ82, L4ROM
3, KJ72 side	K1/K2 remote set	KJ72L5	KJ72, KJ81, L5ROM

4. Data link hardware

4.1. Hardware for KJ71

(1) Configuration

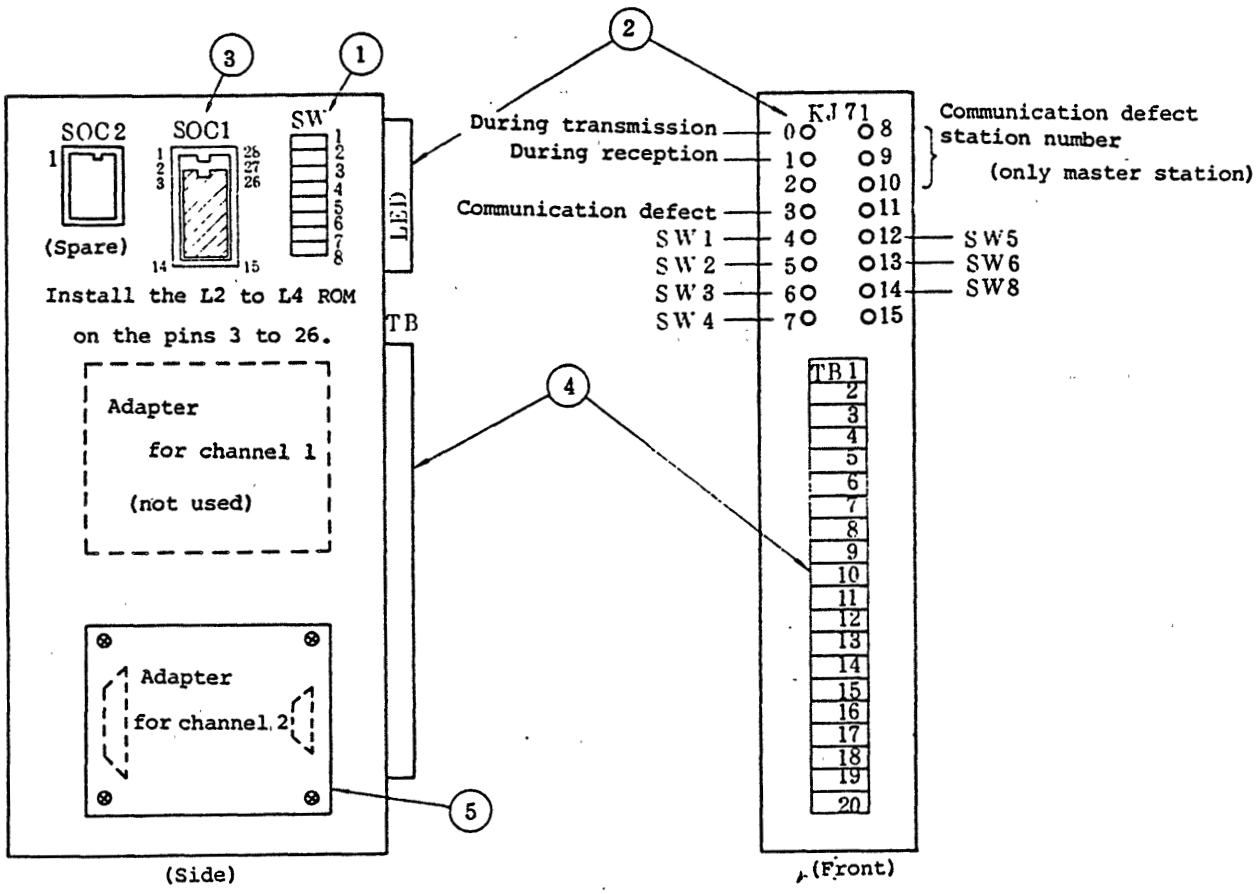
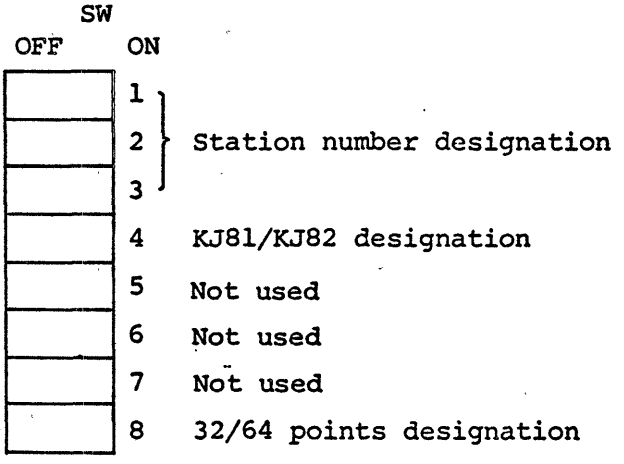


Fig. 4.1 Hardware configuration for KJ71

(2) Switch setting method ①

Execute setting according to the application as shown below.

Table 4.1 KJ71 switch setting



Refer to table 5.2

Master station	Local station 1	2	3	4	5	6	7	Computer link	Remarks
OFF	ON	OFF	ON	OFF	ON	OFF	ON		
OFF	OFF	ON	ON	OFF	OFF	ON	ON		
OFF	OFF	OFF	OFF	ON	ON	ON	ON		
ON	ON	ON	ON	ON	ON	ON	ON		
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		Not used
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		

As slide switches are used, they must be operated so that they are sufficiently on the ON or the OFF side respectively. After setting, the protective cover must be installed.

This cover serves for protection against entry of foreign matter and against change of the switch setting by vibrations.

(3) LED display contents ②

Table 4.2 KJ71 LED display contents

LED No.	Master station	Local station	Computer link	Remarks
LED 0	Transmitting	Transmitting	Not used	Lit darkly during transmission and reception via the link adapter KJ81.
1	Receiving	Receiving	Not used	
2	Not used	Not used	Not used	
3	Communication defect	Communication defect	Not used	Lights up when a communication defect is detected.
4	SW1	SW1	SW1	Indication of the switching condition of SW1 to SW4. (Lit with SW ON)
5	SW2	SW2	SW2	
6	SW3	SW3	SW3	
7	SW4	SW4	SW4	
8	Communication defect station	Not used	Not used	When the master station detects local station trouble, the binary code for the last detected station number is displayed.
9		Not used	Not used	
10		Not used	Not used	
11	Not used	Not used	Not used	
12	SW5	SW5	SW5	The set condition for SW5, SW6, and SW8 is displayed. (Lit for SW ON.)
13	SW6	SW6	SW6	
14	SW8	SW8	SW8	
15	During reception monitoring	Not used	Not used	Lights during reception monitoring check.

(4) ROM installation method ③ SOC1

Confirm that the following ROM has been installed in SOC1. The socket SOC2 is not used.

Table 4.3 ROM installation for KJ71

Master station	Local station	Computer link
L2ROM	L3ROM	L4ROM

In case of ROM exchange, take care to install in the correct direction. As the socket has 28 pins, use the pins 3 to 26 for installation as shown in Fig. 4.1③.

(1) Do not bend the leads at the time of insertion into the socket and at the time of removal from the socket.

(2) Avoid touching of the lead part.

(3) Take care that sweat, oil, etc. does not get onto the glass part or the lead part.
If sweat, oil, etc. has become attached, remove it with alcohol.

(4) Never place a ROM onto metal with leakage or the possibility of leakage.

(5) Never place a ROM onto wood, plastic, vinyl, fibers, electric wires, or paper charged with static electricity.

(5) External wiring method ④

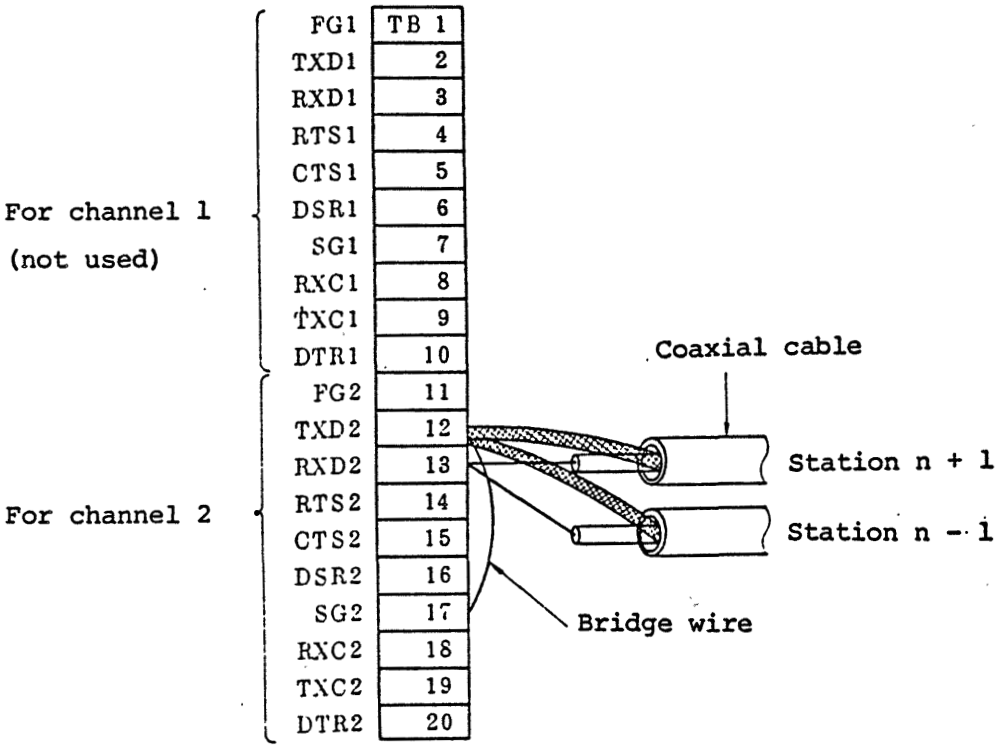


Fig. 4.2 External terminal block of KJ71

When the high-speed link adapter (KJ81) is used, execute external wiring as shown above.

The noise resistance can be improved by connecting TXD2 (TB12) and SG2 (TB17) with a bridge wire.

For use of the RS-232C adapter (KJ82), refer to the computer link system of item 5.6.

(6) Adapter installation method ⑤

Adapter installation connectors are provided for 2 channels, but as channel 1 is not used, install the high-speed link adapter (KJ81) or the RS-232C adapter (KJ82) in the lower connector for channel 2. For installation, match the part surfaces. After the installation, fix the adapter sufficiently with the enclosed 4 fixing screws to prevent defective contact from vibrations.

4.2. Hardware for the K0 programmable controller

(1) Configuration

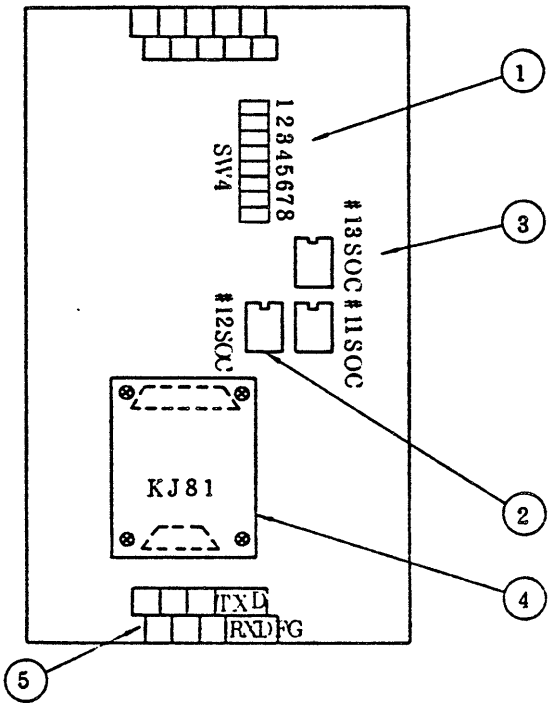
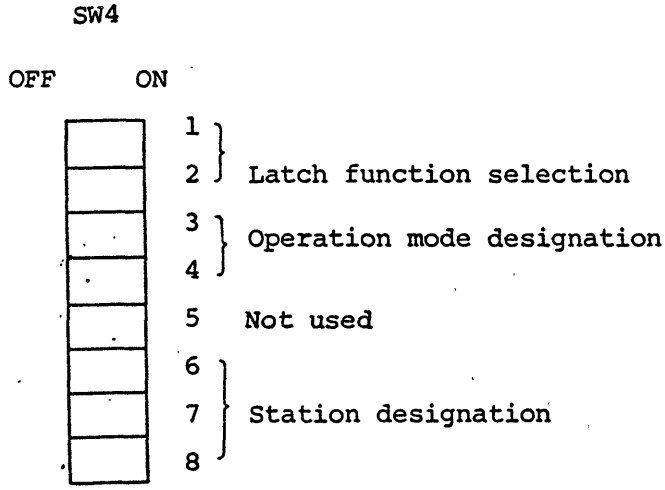


Fig. 4.3 Hardware composition for the K0 programmable controller

(2) Switch setting method ①

Set the operation mode with the switches SW3 and SW4 and the station number with the switches SW6 to SW8 as shown below.

Table 4.4 K0 switch setting



	Single progr. contr.	Remote I/O							Local programmable controller						
		1	2	3	4	5	6	7	1	2	3	4	5	6	7
SW4	Refer to the instruction manual for the K0 programmable controller.														
3	OFF	ON							OFF						
4	OFF	OFF							ON						
5	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
6	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON
7	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON
8	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	ON

As slide switches are used, they must be operated so that they are sufficiently on the ON or the OFF side respectively. After setting, the protective cover must be installed.
This cover serves for protection against entry of foreign matter and against change of the switch setting by vibrations.

(3) ROM and RAM installation method ②, ③

For use of the K0 programmable controller with a remote I/O system or a dispersed control system, specify K0DLS.

The configuration of K0DLS is one L1ROM
one L1RAM
one KJ81.

Install the L1ROM in #12 SOC ②.

Install the L1RAM in #13 SOC ③.

Observe the caution items of page 9 for installation and handling.

(4) Adapter installation method ④

Install the high-speed link adapter (KJ81) by matching the part surfaces. After the installation, fix the adapter sufficiently with the enclosed 4 fixing screws to prevent defective contact from vibrations.

(5) External wiring method ⑤

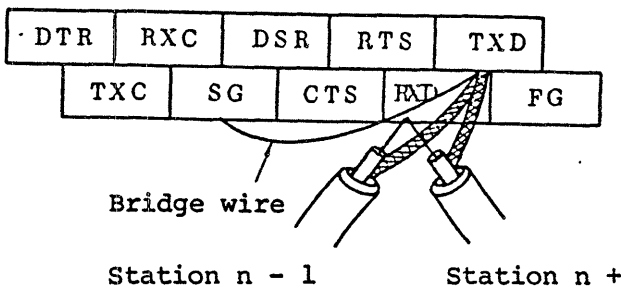


Fig. 4.4 External terminal block of K0

Execute external wiring as shown above.

The external noise resistance can be improved by connecting TXD and SG with a bridge wire.

4.3. Hardware for the high-speed link adapter (KJ81)

(1) Configuration

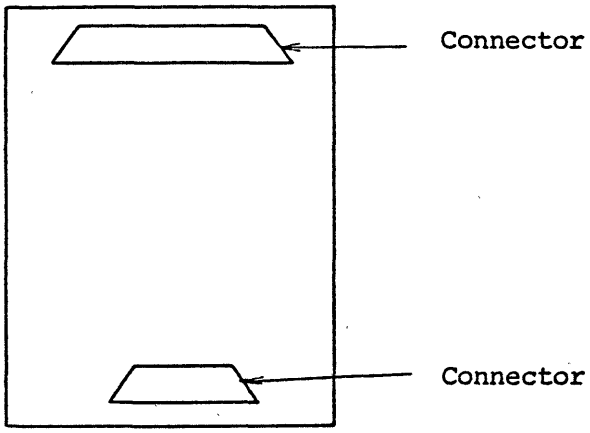
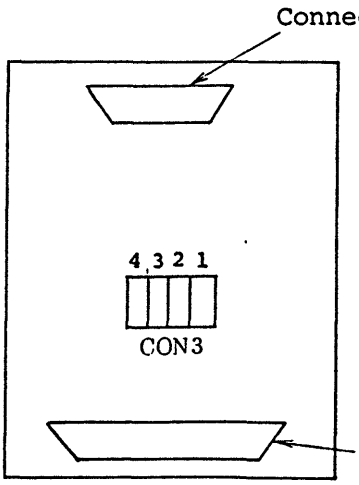


Fig. 4.5 Hardware configuration for KJ81

This is the adapter for reception and transmission at high speed (250 KBPS), and it is used installed in KJ71, KJ72, and K0 unit. (There are no switches for setting.)

4.4. Hardware for the RS-232C adapter (KJ82)

(1) Configuration



This is the RS-232C interface adapter, and it is used installed in the connector for channel 2 of KJ71 for system 6.

Fig. 4.6 Hardware for KJ82

(2) Clock Baud rate switching for transmission and reception by CON3

Refer to the transmission specifications of item 5.6.3.

4.5. Hardware for KJ72

(1) Configuration

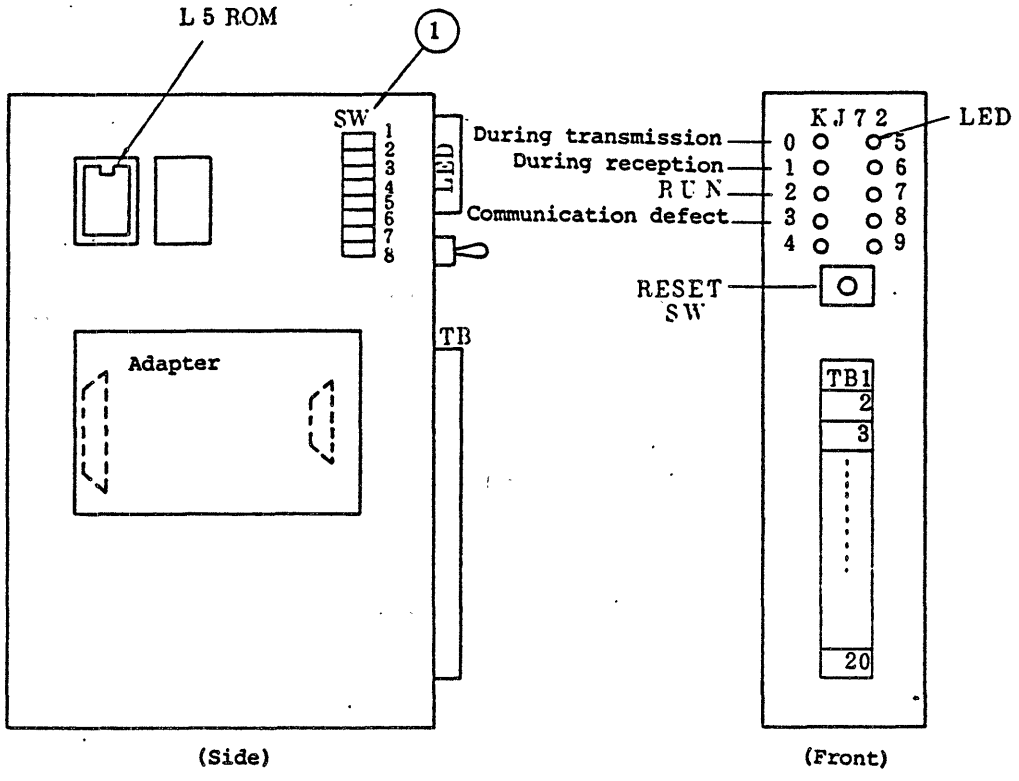
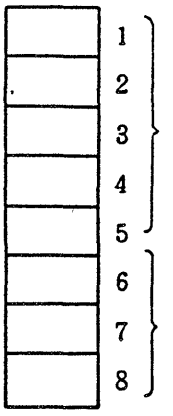


Fig. 4.7. Hardware configuration for KJ72

(2) Switch setting method ①

Execute switch setting according to the application as shown below.

Table 4.5 Switch setting for KJ72



Station No.	1	2	3	4	5	6	7
	OFF (not used)						
	ON	OFF	ON	OFF	ON	OFF	ON
	OFF	ON	ON	OFF	OFF	ON	ON
	OFF	OFF	OFF	ON	ON	ON	ON

As slide switches are used, they must be operated so that they are sufficiently on the ON or the OFF side respectively. After setting, the protective cover must be installed.
This cover serves for protection against entry of foreign matter and against change of the switch setting by vibrations.

(3) External wiring method

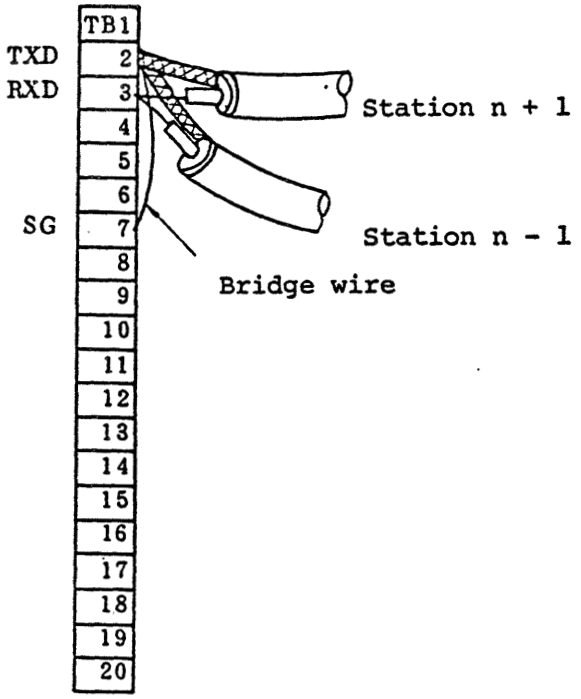


Fig. 4.8 External terminal block for KJ72

(4) LED display contents and switch (RESET SW) handling method

LED0 (transmitting): Lights up during transmission to the master station.

LED1 (receiving): Lights up during reception from the master station. As LED0 and LED1 only light up during transmission or reception respectively, they are lit on the dark side at the time of normal operation.

LED2 (RUN): This lights up when the CPU is operating normally without communication defect.

LED3 (communication defect): This lights up when transmission and reception do not operate normally, and the RUN display goes out.

LED4 (Not used)

LED5 (SW6)
LED6 (SW7)
LED7 (SW8)
} Indication of the set condition of the switches SW6 to SW8 (lit with SW ON)

LED8 (Not used)

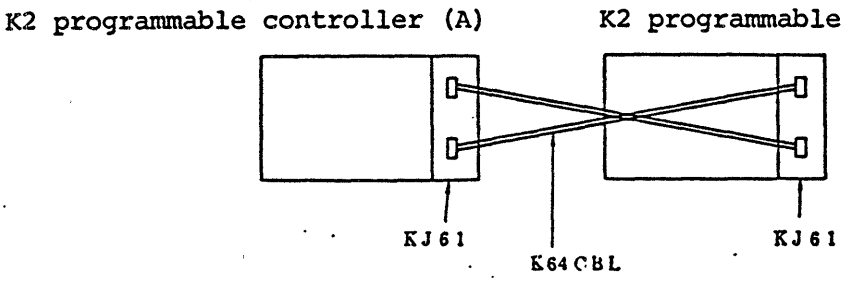
LED9 (Not used)

Switch (RESET): This is used for resetting after a communication defect has occurred. Hardware resetting is executed.

5. Data link system configuration, handling, and programming method

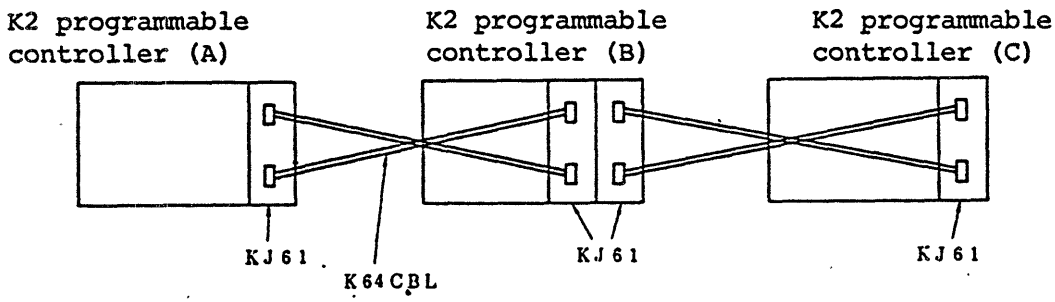
5.1. Parallel data link system between K2s

5.1.1. Configuration



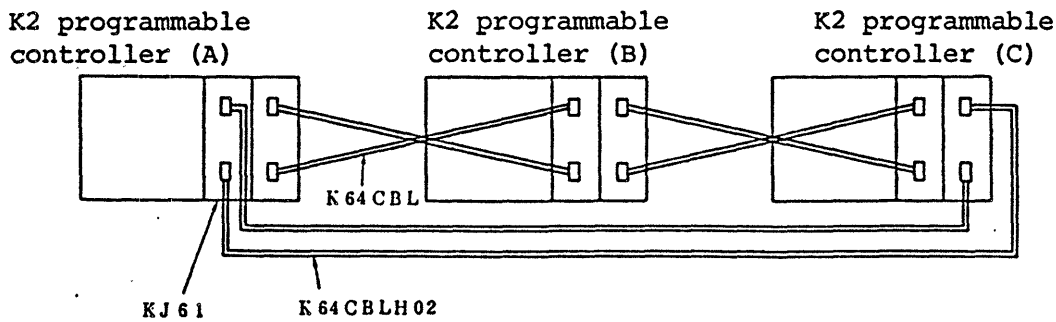
Max. number of I/O points: 992 points

Fig. 5.1 Parallel arrangement of 2 units



Max. number of I/O points: 1,472 points

Fig. 5.2 Parallel arrangement of 3 units (A)



Max. number of I/O points: 1,440 points

Fig. 5.3 Parallel arrangement of 3 units (B)

5.1.2. Specifications

(1) Number of linkable signal points

Max. 128 points.
Setting of signal input or output can be executed in units of 16 points.
(Setting is possible with the DIP switches on the KJ61 card. Refer to item 5.1.3.(1).)

Note: The above specification for the possible number of linkable signal points applies for one KJ61 card, but this will not be doubled when two KJ61 cards are used.
(Limitation to max. 128 points exists because of the CPU specifications.)

(2) Link signal I/O number

The 128 points from Y00 to Y7F are used.
Accordingly, principally only input units can be connected to the basic base K28B (00 to 7F). (This applies for all programmable controllers.)

Note: When the external trouble monitor unit KN62 or an output unit is installed, link use for Y00 to Y7F becomes impossible, so that the number of linkable points is reduced accordingly.

Example:

When KN62 is inserted into No. 1 (on the right of the K2CPU) of the basic base K28B, the number of linkable points becomes max. 112 points from Y10 to Y7F.

(3) KJ61 installation position

KJ61 can be installed in any position on the extension base K68B.
Max. two KJ61 can be installed for one programmable controller.
Accordingly, linkage is possible for up to three programmable controllers.

Note: As one KJ61 is considered as an I/O card with 16 points, the max. number of process I/O points per K2CPU becomes 512 - 16 = 496 points.

(4) External dimensions

The I/O units for K1 and K2 have the same dimensions.

(5) Length of the KJ61 connection cable

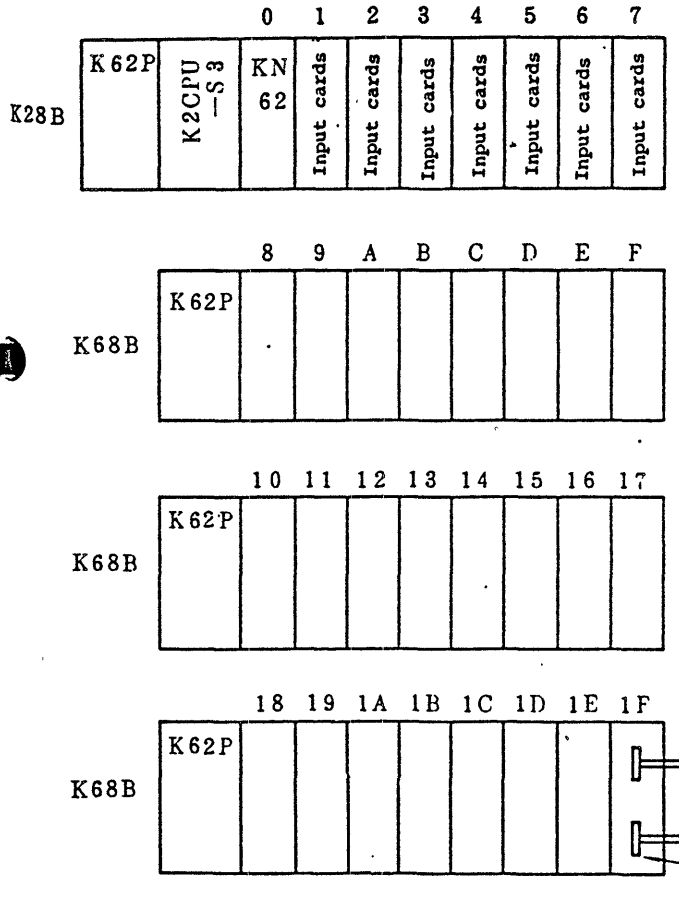
1 m (K64CBL)

3 m (K64CBLH02)

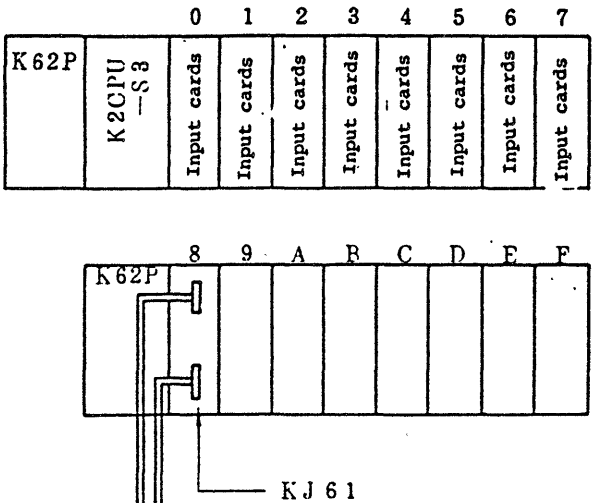
5.1.3. Link examples

(1) Example for linkage of two programmable controllers

Programmable controller A (A.PC)

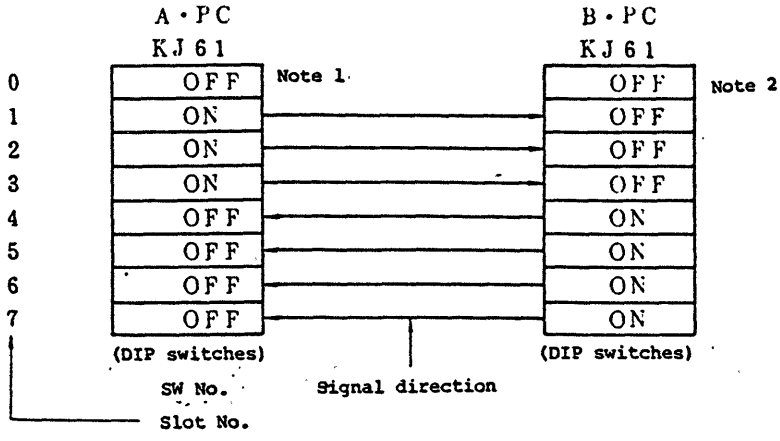


Programmable controller B (B.PC)



In the above figure, KJ61 can be inserted at any position of the extension base.
As KN62 is inserted into slot 0 of the A.PC in the example of the above figure, Y00 to Y0F can not be used for linkage.
Explanations will be given for use of the 48 points from Y10 to Y3F for output (A to B) and use of the 64 points from Y40 to Y7F for input (B to A).

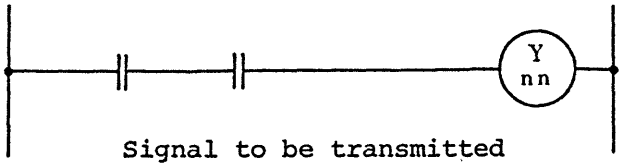
KJ61 I/O designation method



Note 1: Output with ON, input with OFF.

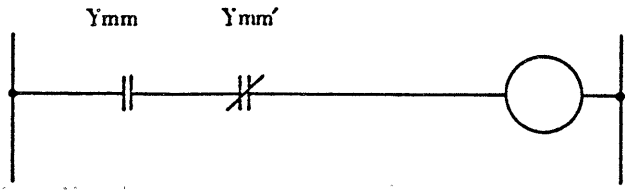
Note 2: As KN62 is inserted into slot 0, this can not be used for linkage. (Both switches to be set to OFF.)

Signal transmission method from A.PC to B.PC



Note 1: nn is any number from 10 to 3F, and output is executed as a coil.

Method for use of the signal from the B.PC to the A.PC by the A.PC

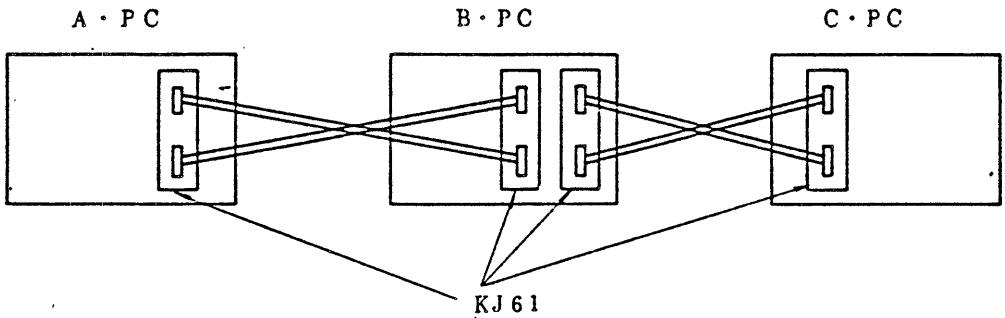


Note 2: Ymm and Ymm' are any number from 40 to 7F, and use is possible in the same way as for a normal contact.

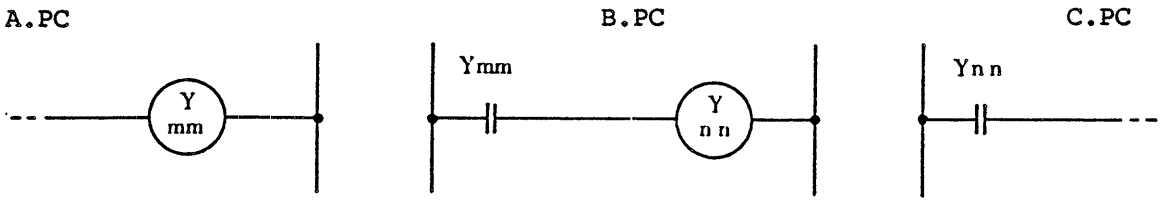
Note 3: After execution of the END instruction, Ynn is transmitted continuously from the A.PC to the B.PC, and Ymm and Ymm' are transmitted continuously from the B.PC to the A.PC.

(2) Example for linkage of three programmable controllers

(2)-1. Use of four KJ61

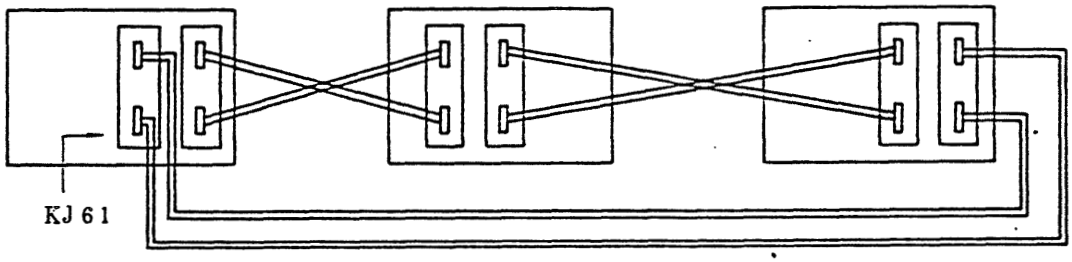


The total number of linkable signal points is 128 points.
Exchange of signals between the A.PC and the C.PC must be relayed as follows by the program of the B.PC.



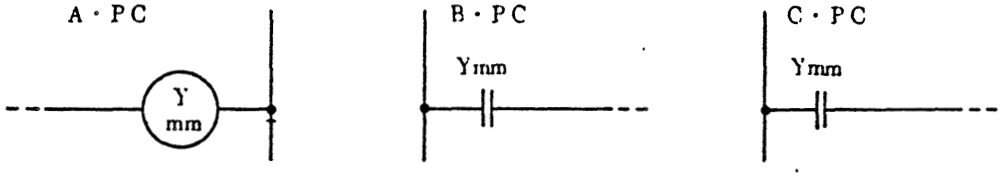
The Ymm output of the A.PC is used as Ynn for the C.PC.

(2)-2. Use of six KJ61



(1) The total number of linkable signal points is 128 points.

(2) In the case of the above figure, the output of one programmable controller is put out simultaneously to both other programmable controllers.



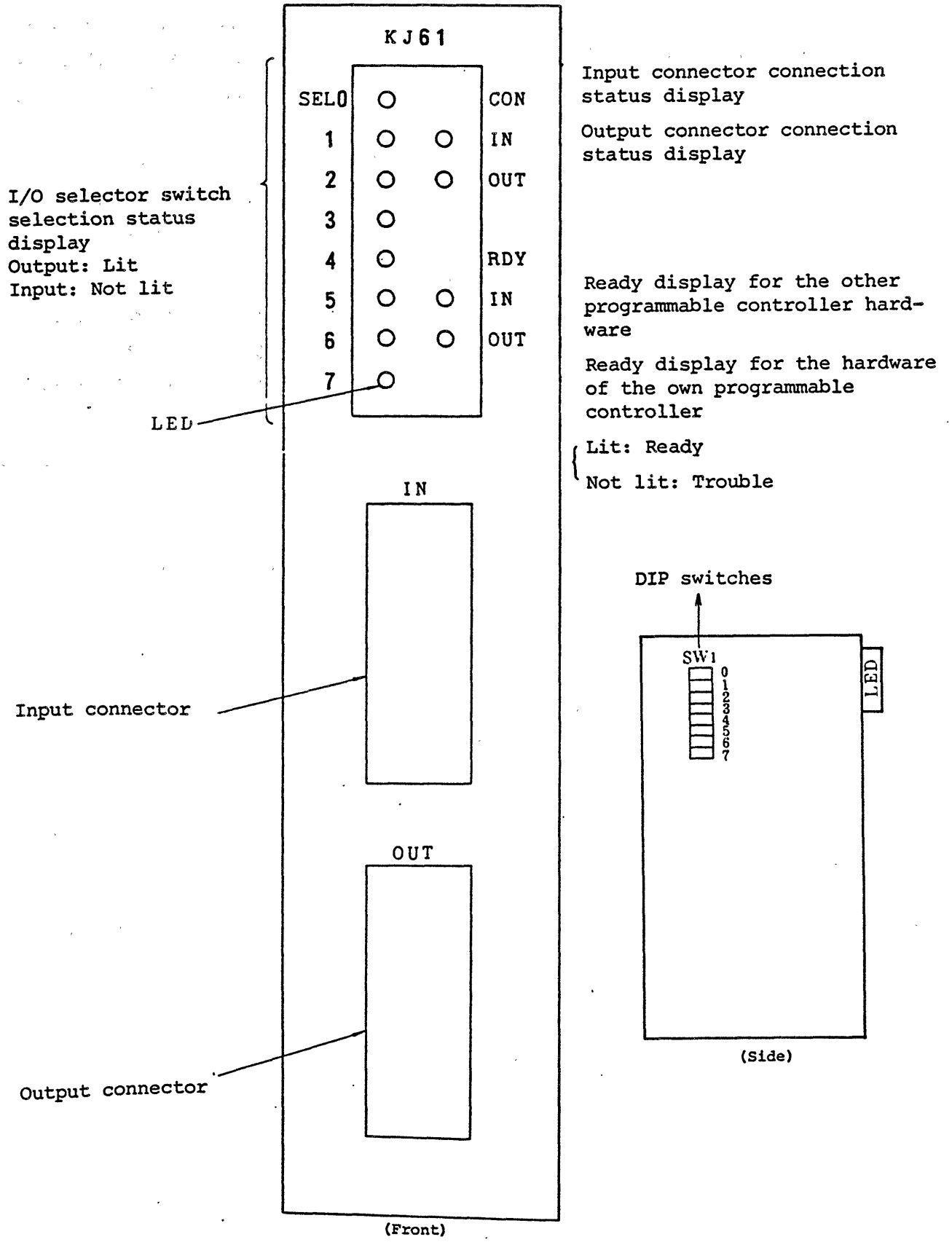
Ymm can be used freely by B.PC and C.PC.

5.1.4. Special notes

(1) For use of KJ61, the K2CPU must be a K2CPU-S2 or a K2CPU-S3. KJ61 can not be used with a standard K2CPU.
However, K2CPU-S2 and K2CPU-S3 have higher level compatibility with the K2CPU, so that they can be used for applications for which the K2CPU was used until now.

5.1.5. Handling

(1) Card arrangement and meaning



(2) Caution items for K2CPU-S2/S3 power ON and RUN-STOP switch operation

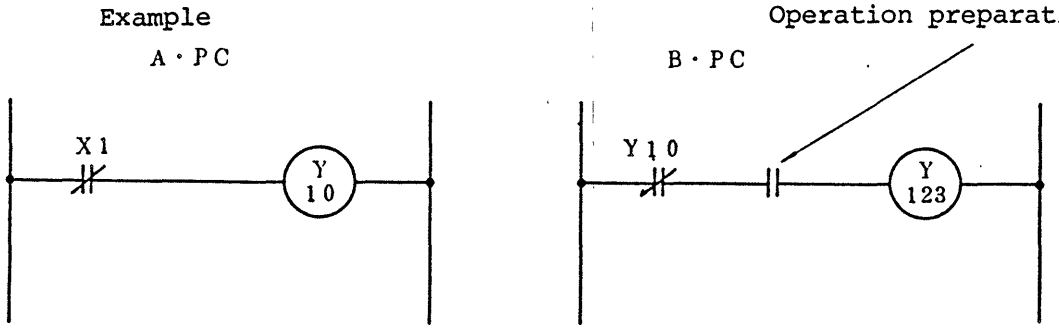
(2)-1. When KJ61 is inserted into the K2CPU-S2/S3, sequence processing (scanning) will not be started even with the RUN-STOP switch set to RUN when the hardware of the opposite programmable controller is not ready at the time of power ON.
Accordingly, the RUN display lights up, but the RUN output of M255 remains OFF. Sequence processing will be started when the hardware of the opposite programmable controller is ready.

(2)-2. When the RUN-STOP switch of the opposite programmable controller is set to STOP, hardware ready for the opposite programmable controller becomes OFF, and the RUN display flickers to indicate trouble. The process output of the programmable controller on this side naturally becomes OFF.

(2)-3. Link data output from the programmable controller on this side to the one on the opposite side is executed collectively after execution of the END instruction. (Naturally, this is executed only for the data for which the I/O designation "Output" has been selected.
When there are two opposite programmable controllers, the same data will be put out simultaneously to both.
Reception of the link data from the opposite programmable controller will be executed even during RUN.

(2)-4. At the time of power ON, all link data become OFF.
Accordingly, as all link data become OFF for the scanning time of CPU 1 until execution of the END instructions, considerations must be made for the program when this presents problems.

Example



In the above circuit, Y123 may become ON momentarily at the time of power ON even when X1 is OFF.

Countermeasure: Insert operation preparation conditions etc. as shown above.

(3) Trouble detection contents in regard to KJ61, confirmation, and resetting method

(3)-1. There are the following 3 trouble detections in regard to KJ61.

a) Hardware ready on the opposite side (Trouble number 5001)

Causes for occurrence:

(i) Hardware trouble on the opposite side

(ii) Defective connection cable (wire break, defective contact, etc.)

(iii) The RUN-STOP switch on the opposite programmable controller is set to STOP.

(iv) Resetting has been executed with the reset switch of the programmable controller on the opposite side.

b) KJ61 I/O designation defect (1) (Trouble number 5002)

Cause for occurrence

o The programmable controller on this side has two KJ61 installed and the selection contents differ. (The selection contents for both KJ61 must coincide.)

c) KJ61 I/O designation defect (2) (Trouble number 5003)

Cause for occurrence

o While the output side for KJ61 has been selected for the programmable controller on this side, the output side for KJ61 also has been selected for the programmable controller on the opposite side, and data are being transmitted from the programmable controller on the opposite side. (Output designation may be made only for one side.)

(3)-2. Trouble confirmation method

The RUN lamp flickers in case of the troubles a), b), and c). Use the following methods to confirm the trouble number for the defects a), b), or c).

o Confirmation by K6PU/K7PU

o Confirmation by K6PU/K7PU

(3)-3. Resetting method

After removal of the trouble causes listed in item (3)-1, execute resetting according to one of the following methods.

o Method by power supply resetting

(i) Set the power switch of both programmable controllers once to OFF.

(ii) Set the RUN-STOP switch of both programmable controllers to RUN.

(iii) Set the power switch of both programmable controllers again to ON.

o Method using the programmable controller reset switch

(i) Set the RUN-STOP switch of both programmable controllers to RUN.

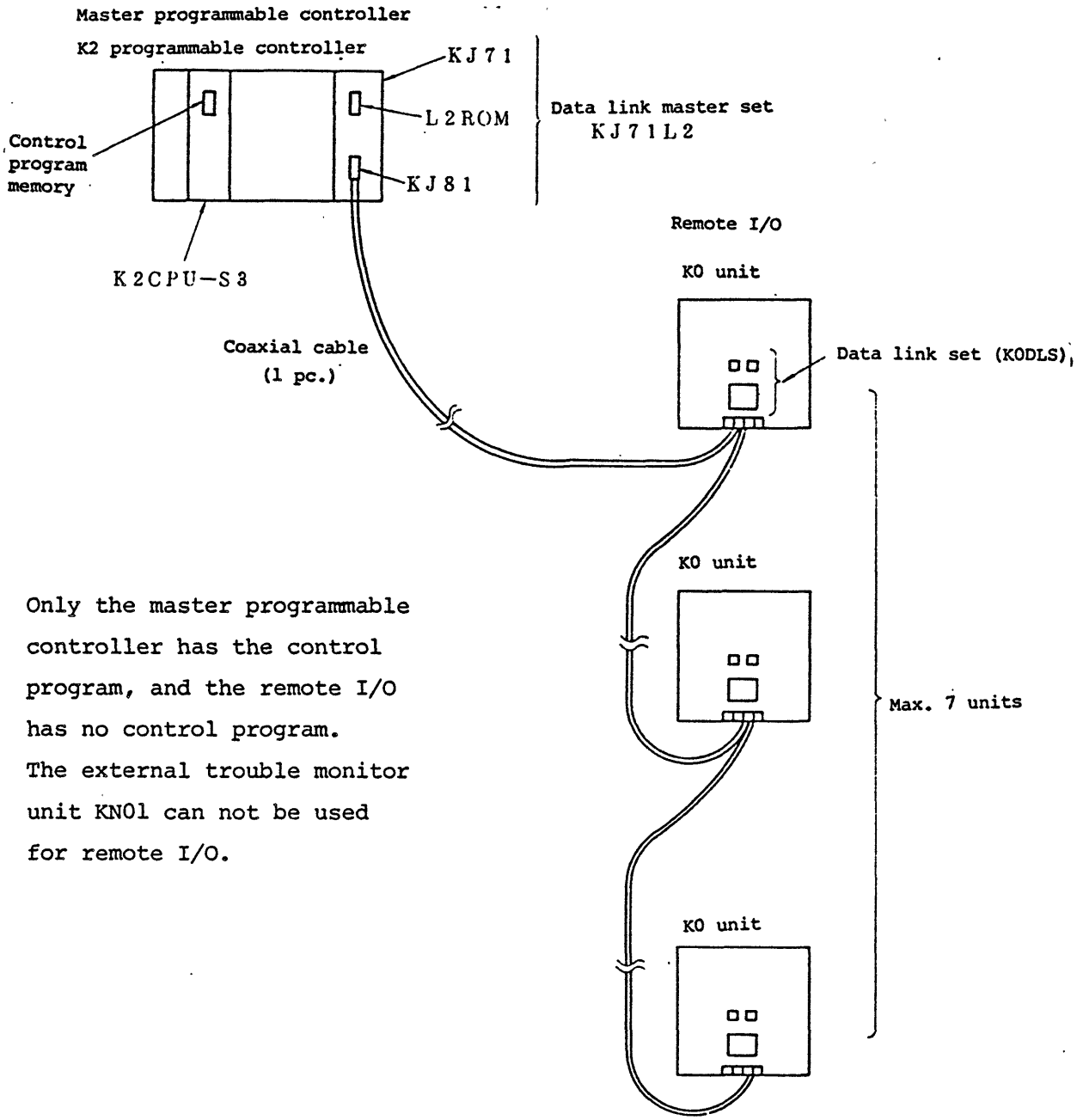
(ii) Execute resetting with the reset switch of both programmable controllers. (This must be executed for both programmable controllers.)

Note:

Please note that the RUN display will not flicker in case of hardware ready trouble on the opposite side with the first ready after power ON for the programmable controller.
(As described in item (2), waiting for ready of the opposite programmable controller will be executed.)
Accordingly, when no operation is executed although the RUN display lights at the time of power ON (no RUN output of M255), confirm the KJ61 RDY display.

5.2. Remote I/O system by K2 and K0 unit

5.2.1. Configuration



Only the master programmable controller has the control program, and the remote I/O has no control program.
The external trouble monitor unit KN01 can not be used for remote I/O.

Fig. 5.4 Remote I/O system with K2 and K0

5.2.2. Specifications

(1) Number of remote I/O units (K0 units): Max. 7 units.

(2) Number of I/O points

Max. 480 points total for remote I/O units and master I/O unit (512 points - 32 points)

(3) Transmission speed between K2CPU and remote I/O: 250 KBPS (bit/sec)

Note: As the transmission control between K2CPU and remote I/O is executed by the CPU in the KJ71, the sequence operation time practically is not influenced.

(4) Overall coaxial cable length: Max. 500 m

5.2.3. Program method

The program method will be explained according to the following configuration diagram.

Master programmable controller

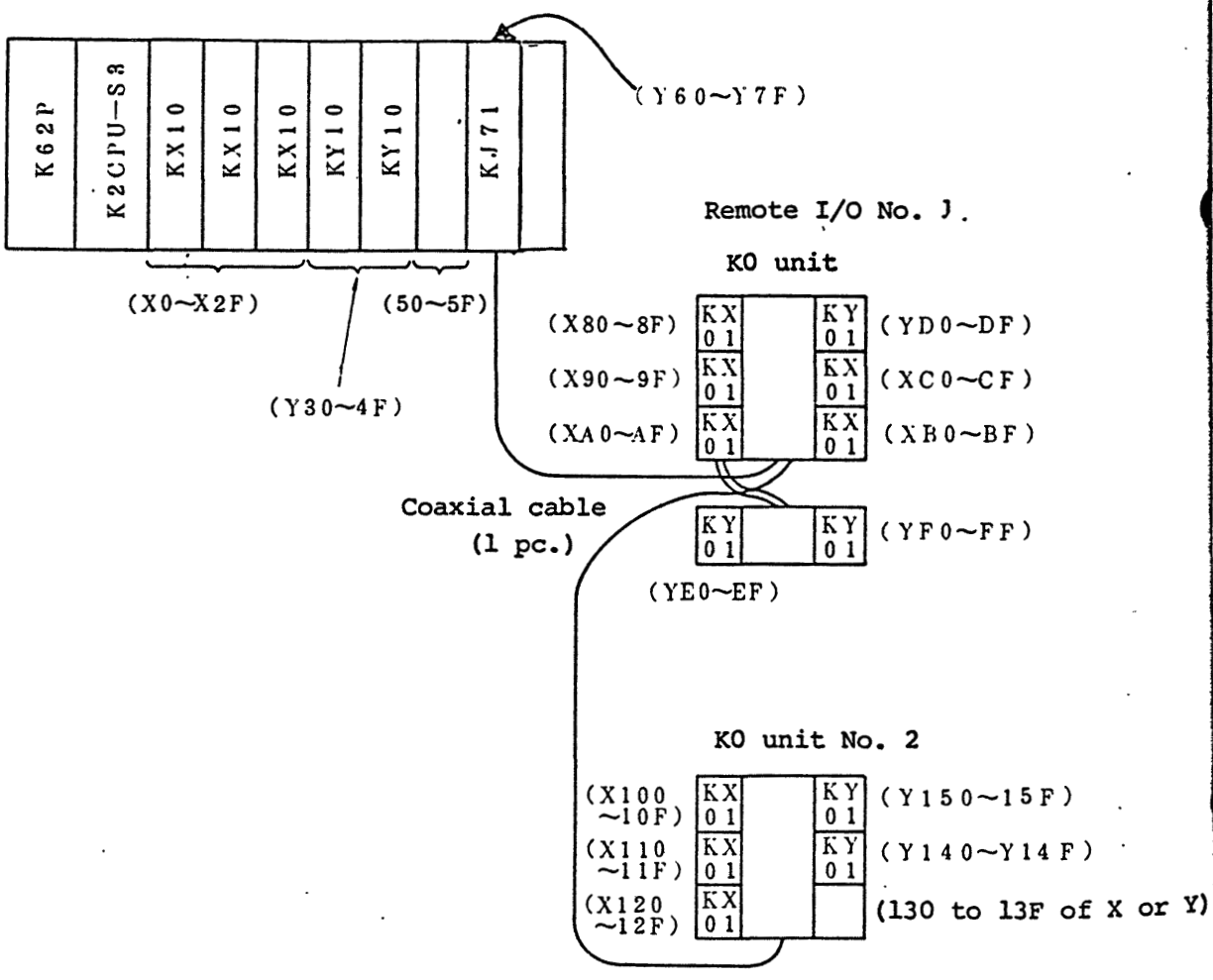


Fig. 5.5 Remote I/O configuration example with K0

(1) The I/O numbers become as shown in the brackets in Fig. 5.5.

Notes:

1) It is recommended to insert KJ71 into the last position of the K2 system.

2) It is recommended to allot the I/O numbers in the sequence of master side I/O, KJ71, remote I/O unit No. 1, and remote I/O unit No. 2.

3) In the above figure, the remote I/O after Y7F is X80, but numbers may be jumped.
For example, the remote I/O No. 1 may start with X100.
Jumping of numbers between the remote I/O No. 1 and the remote I/O No. 2 also is possible.

4) For the I/O units in the remote I/O, use the input units first and then the output units.
The numbers in the remote I/O must be consecutive.
Accordingly, X or Y numbers should be taken for the empty area.

5) Use of only input units or only output units for the I/O units in the remote I/O also is possible.

(2) When the I/O numbers in the brackets have been taken, insert the following initial program at the start of the K2 programmable controller program. (Designation of the I/O data link range.)

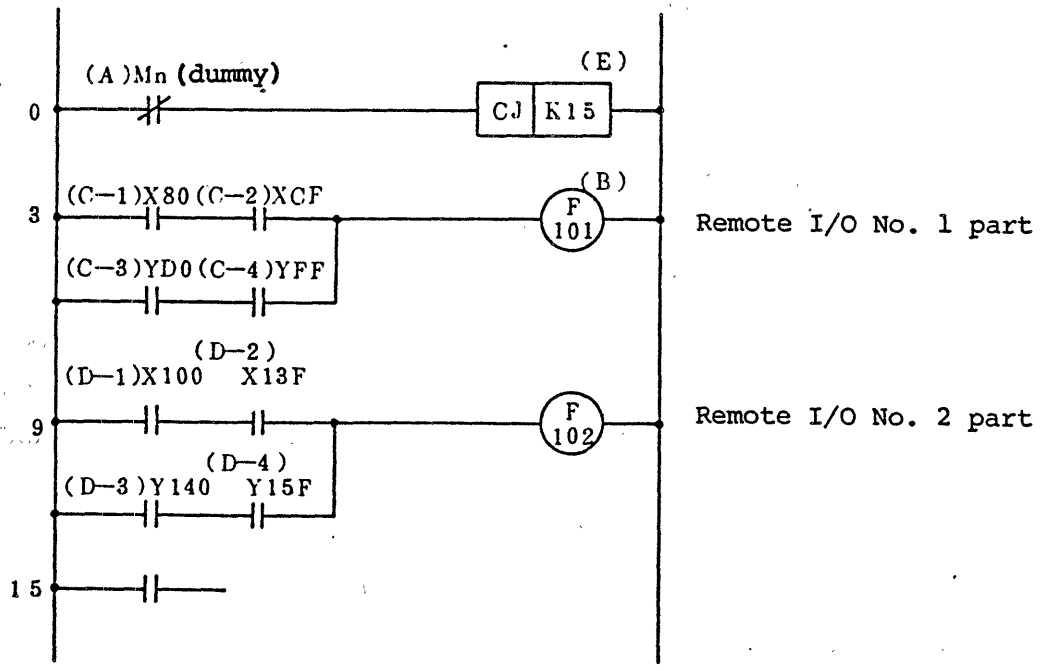


Fig. 5.6 Initial program

Note:

The above initial program serves to designate the remote I/O link range and has no meaning for the sequence, but the format shown in Fig. 5.6 should be used.

(A) Mn: Not used temporary memory (dummy)

(B) The 1 of the lower digit of the coil F101 indicates the remote I/O No. 1.
Accordingly, the numbers are from F101 to F107, and numbering must be started from F101.

(C-1) X80 indicates the leading input number of No. 1 as seen from the master programmable controller. Take care that this leading number does not overlap with the final allotment number of the master programmable controller.

(C-2) XCF indicates the last input number of No. 1 as seen from the master programmable controller. In any case, the leading end shall be "0" and the final end shall be "F". (Designation must be executed in units of 16.)

(C-3) YDO indicates the leading output signal number to No. 1 as seen from the master programmable controller.

(C-4) YFF indicates the final output signal number to No. 1 as seen from the master programmable controller. Use continuous numbers for (C-2) and (C-3).

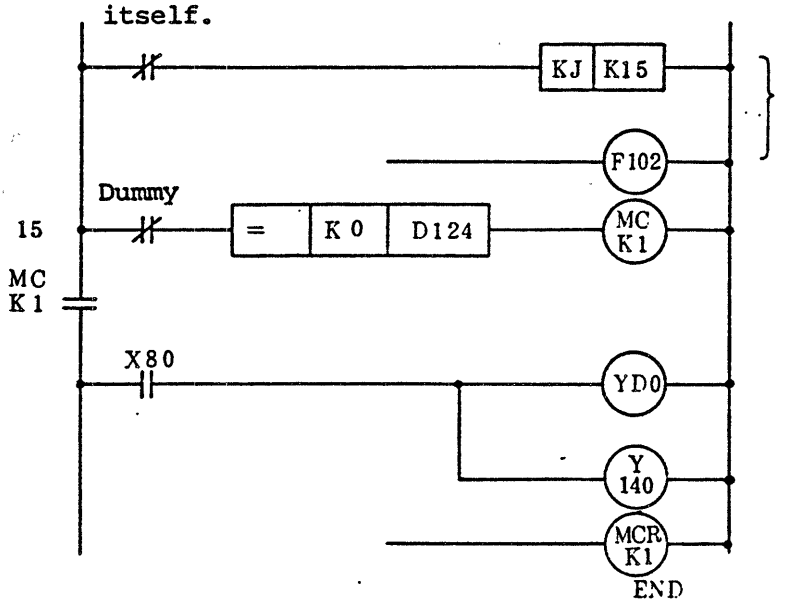
(D-1) to (D-4) These are the allotment designations the same as for No. 1 as seen from the master programmable controller. Numbers may be jumped between (C-4) and (D-1). When for example only input signals are used for No. 1, the program designation for (C-3) and (C-4) is not required.

(E) The CJ jump destination in the example is the step No. following OUT F102.

(3) Program method (master programmable controller)

Start the program after the initial program of Fig. 5.6.

The program method is the same as for a program for the K2 by itself.



Initial program
Refer to Fig. 5.6

Sequence program
YD0 of No. 1 becomes ON by X80 ON of No. 1. Y140 of No. 2 also becomes ON.

Fig. 5.7 Program example

Notes:

1) There is no sequence program for the remote I/O No. 1 to No. 7 of the remote I/O system.

2) When the power supply of a remote I/O station is interrupted, or when trouble occurs in the transmission system, the trouble station is stored in the data register D124 as shown in table 5.1. When all stations are normal, D124 = 0 exists. Insert the MC K1 program at the start so that this sequence program becomes ineffective when trouble has occurred for even one station.

3) When a KJ71 series data link control unit has been inserted into the master station K2CPU, the initial program of Fig. 5.6 must be specified at the start, as otherwise the RUN display of the programmable controller (K2CPU-S3) will flicker. ("5007" will be displayed with readout by TEST - K - STEP (+) of the PU.)

5.2.4. Hardware setting for master programmable controller and remote I/O

(1) Master programmable controller

In KJ71

(1) Installation of the high-speed link adapter KJ81

Confirm installation in the socket for channel 2 of Fig. 4.1.(5). Install with matching part surfaces and fix with the 4 fixing screws.

(2) L2ROM installation

Confirm installation in SOC1 of Fig. 4.1.(3).

(3) Master station selection

Execute setting according to table 4.1. The LEDs of Fig. 4.1. light up after energization.

(4) Installation on the body base

After installation, fix with the 2 fixing screws.

Note: Refer to item 8 for external wiring execution.

(2) Remote I/O

In the K0 programmable controller

(1) Installation of the high-speed link adapter KJ81

Install in the position of Fig. 4.4.(4).
Install with matching part surfaces and fix with the 4 fixing screws.

(2) L1ROM installation

Install in SOC #12 of Fig. 4.4.(2).
Pay sufficient attention not to mistake the pin numbers (pin 1 is at the left top).

(3) L1RAM installation

Install in SOC #13 of Fig. 4.4.(3).

Pay sufficient attention not to mistake the pin numbers (pin 1 is at the left top).

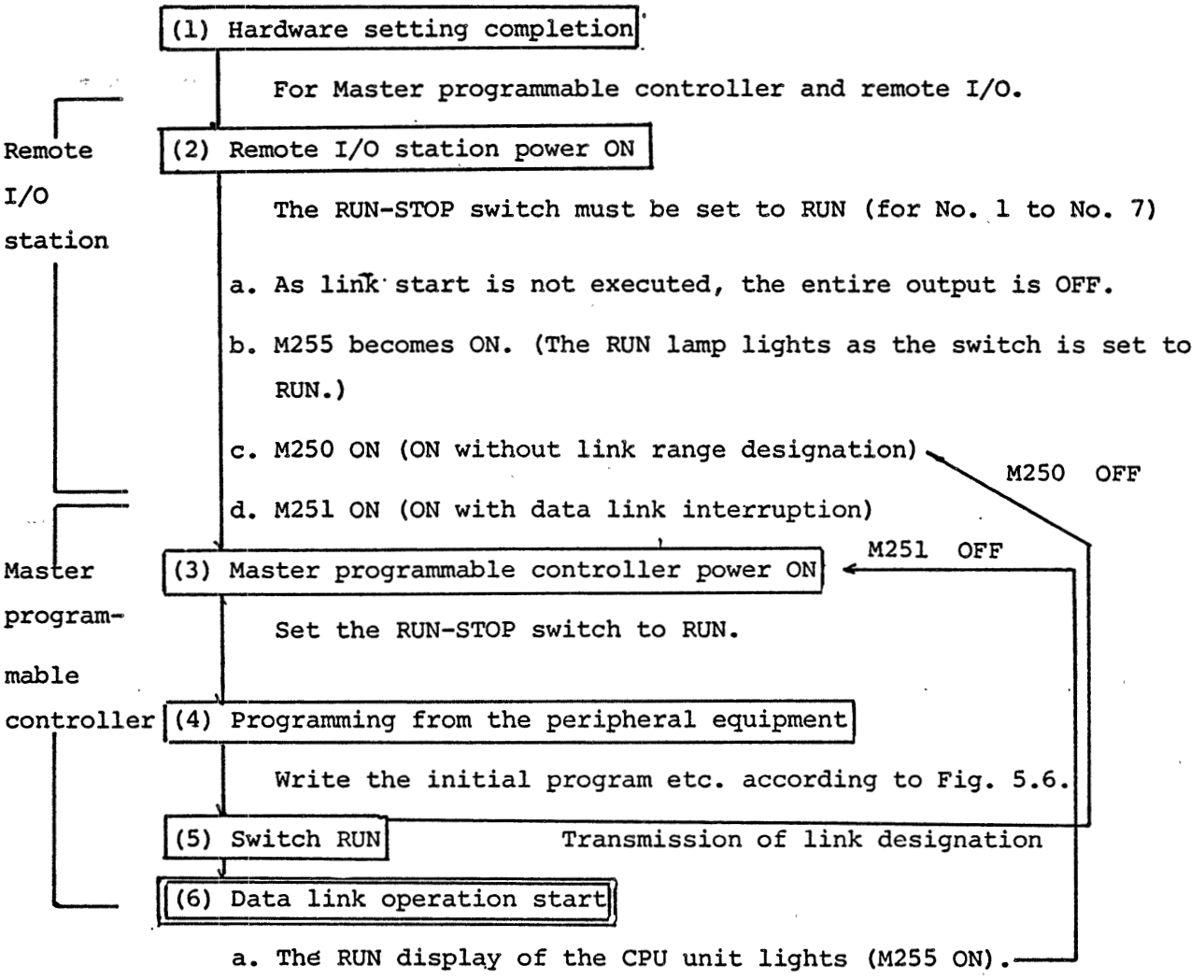
(4) Station number and operation mode selection

Execute setting according to table 4.4.

Note: Refer to item 8 for external wiring execution.

5.2.5. Operation sequence

(1) Operation start



b. The transmission and reception lamps LED1 and LED2 of the KJ71 unit light darkly.

Note: The power ON sequence principally should be started with the remote I/O stations and then should proceed to the master programmable controller. (When the programming for the master programmable controller has been completed, simultaneous power ON also is possible.)

(2) Operation stop

Execute operation stop basically in the reverse order of operation start.

When the RUN-STOP switch of the master programmable controller is set to STOP, the master programmable controller will stop, and as transmission and reception will be interrupted, M251 of the remote I/O stations will become ON, and output will become OFF for all points.

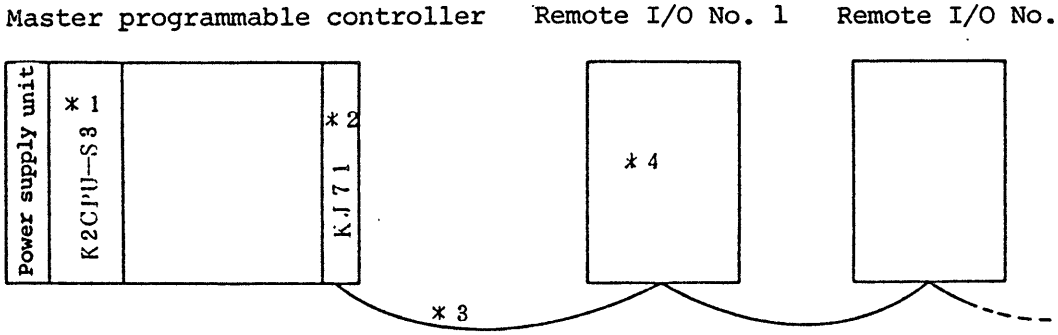
Operation restart will be executed when the RUN-STOP switch of the master programmable controller again is set to RUN.

(3) Remote I/O station parallel off

As the remote I/O are only a system for remote I/O of the master programmable controller, parallel off operation is not possible. Accordingly, the RUN-STOP switches should be set to RUN before power ON. Switching to STOP after power ON is prohibited.

* Parallel off: Removal from data link condition.

5.2.6. Trouble contents and treatment



The trouble contents largely can be divided as follows.

*1: Trouble in the K2CPU-S3

*2: Trouble in the KJ71 unit

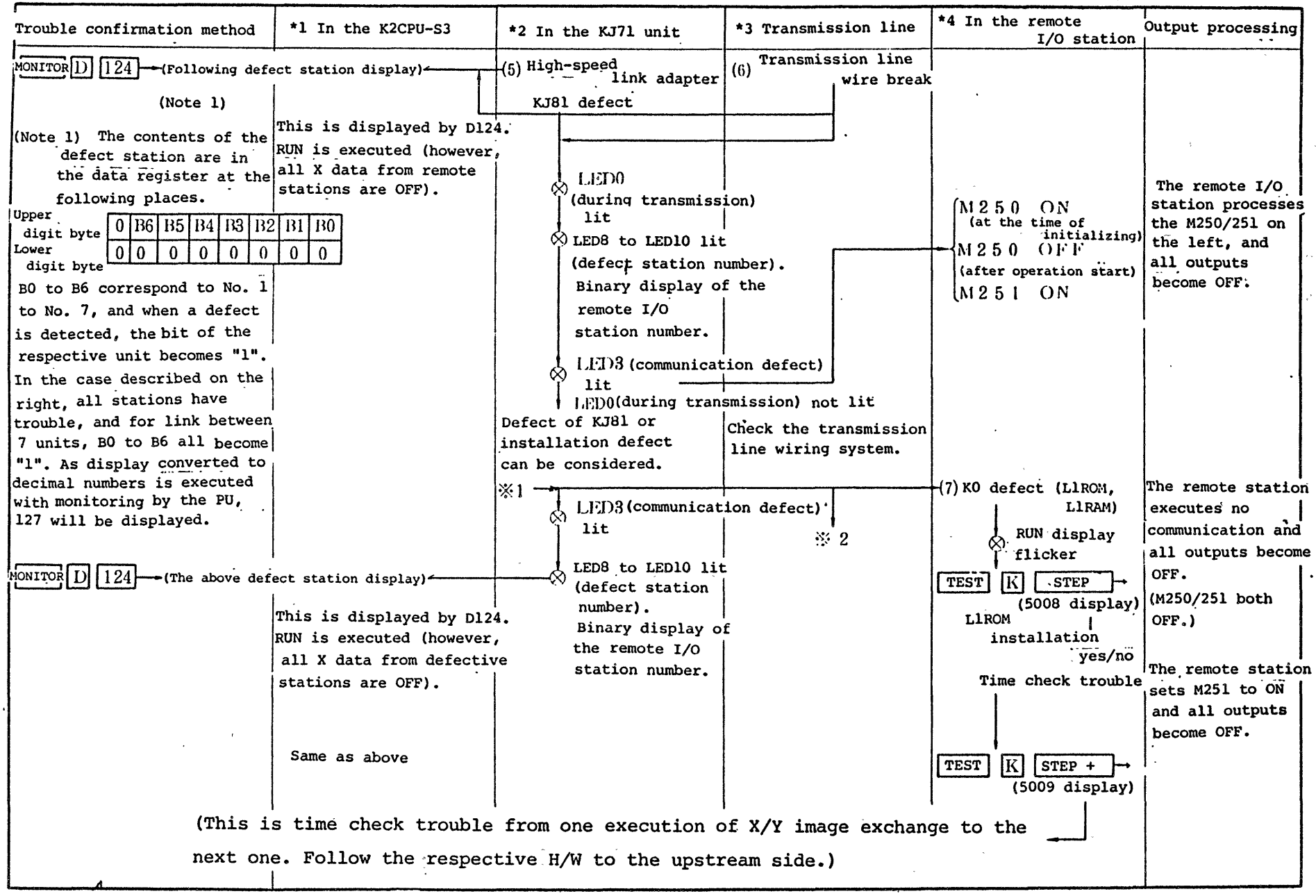
*3: Transmission line trouble

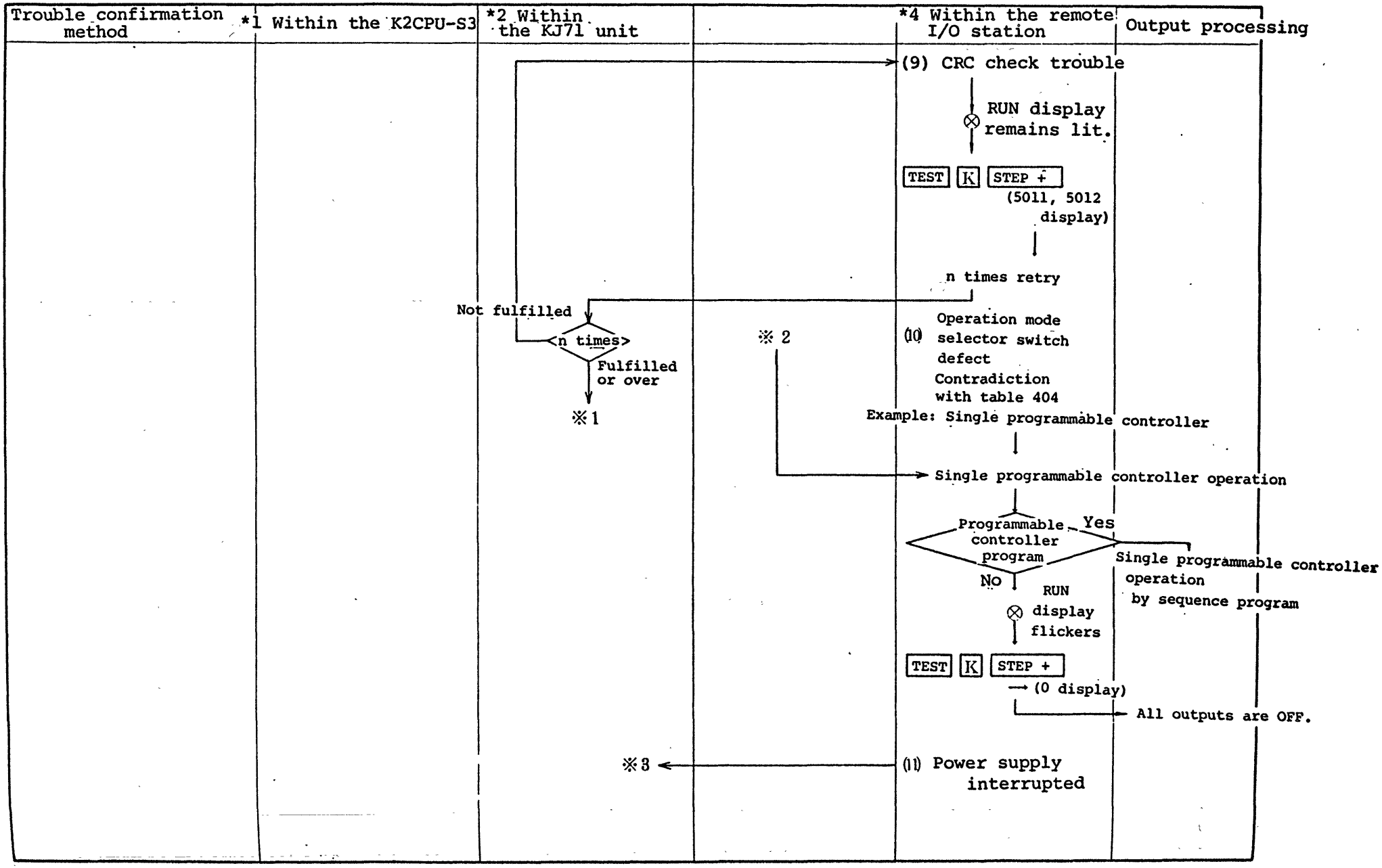
*4: Trouble in the remote I/O station

The various trouble contents as well as confirmations and treatment are described in the following (in regard to linkage).

Table 5.1 Trouble contents and their treatment

Trouble confirmation method	＊1 K2CPU—S3	*2 Trouble in the KJ71 unit	*3 Transmission line trouble	*4 Trouble in the remote I/O station	Output processing
RUN display flicker ←	(1) Initial program defect			In any of the following cases, the data communications are not started and all outputs remain OFF.	
TEST K STEP + → (5007 display) → Initial program correction (refer to Fig. 5.6)					
Same as above (5004 display) ←		(2) KJ71 overlapping installation			
→ Check if 3 or more cards have been installed.					
Same as above (5005 display) ←		(3) L2ROM installation trouble			
→ Check if there are two KJ71 with installed L2ROM.					
Same as above (5006 display) ←		(4) KJ71H/W (S/W) Trouble			
→ ⊗ LED11 lit					
→ H/W of KJ71 Confirm the ROM installation switch selection contents.					


Trouble confirmation method
*1 In the K2CPU-S3
*2 In the KJ71 unit
*3 Transmission line
*4 In the remote I/O station
Output processing
MONITOR D 124 (Following defect station display)
(Note 1)
(5) High-speed link adapter KJ81 defect
(6) Transmission line wire break
(Note 1) The contents of the defect station are in the data register at the following places.
Upper digit byte 0 B6 B5 B4 B3 B2 B1 B0
Lower digit byte 0 0 0 0 0 0 0 0
B0 to B6 correspond to No. 1 to No. 7, and when a defect is detected, the bit of the respective unit becomes "1". In the case described on the right, all stations have trouble, and for link between 7 units, B0 to B6 all become "1". As display converted to decimal numbers is executed with monitoring by the PU, 127 will be displayed.
This is displayed by D124. RUN is executed (however, all X data from remote stations are OFF).
LED0 (during transmission) lit
LED8 to LED10 lit (defect station number). Binary display of the remote I/O station number.
LED3 (communication defect) lit
LED0 (during transmission) not lit
M250 ON (at the time of initializing)
M250 OFF (after operation start)
M251 ON
The remote I/O station processes the M250/251 on the left, and all outputs become OFF.
Defect of KJ81 or installation defect can be considered.
Check the transmission line wiring system.
※1
※2
(7) K0 defect (L1ROM, L1RAM)
LED3 (communication defect) lit
RUN display flicker
The remote station executes no communication and all outputs become OFF. (M250/251 both OFF.)
MONITOR D 124 (The above defect station display)
LED8 to LED10 lit (defect station number). Binary display of the remote I/O station number.
TEST K STEP → (5008 display)
L1ROM installation yes/no
This is displayed by D124. RUN is executed (however, all X data from defective stations are OFF).
Time check trouble
The remote station sets M251 to ON and all outputs become OFF.
TEST K STEP + → (5009 display)
Same as above
(This is time check trouble from one execution of X/Y image exchange to the next one. Follow the respective H/W to the upstream side.)


Trouble confirmation method
*1 Within the K2CPU-S3
*2 Within the KJ71 unit
*4 Within the remote I/O station
Output processing
(9) CRC check trouble
RUN display remains lit.
TEST K STEP +
(5011, 5012 display)
n times retry
Not fulfilled
<n times>
Fulfilled or over
※1
※2
(10) Operation mode selector switch defect
Contradiction with table 404
Example: Single programmable controller
Single programmable controller operation
Programmable controller program
Yes
No
Single programmable controller operation by sequence program
RUN display flickers
TEST K STEP +
→ (0 display)
All outputs are OFF.
※3
(11) Power supply interrupted

5.3. Remote I/O system with K2CPU and K1, K2 I/O units

5.3.1. Configuration

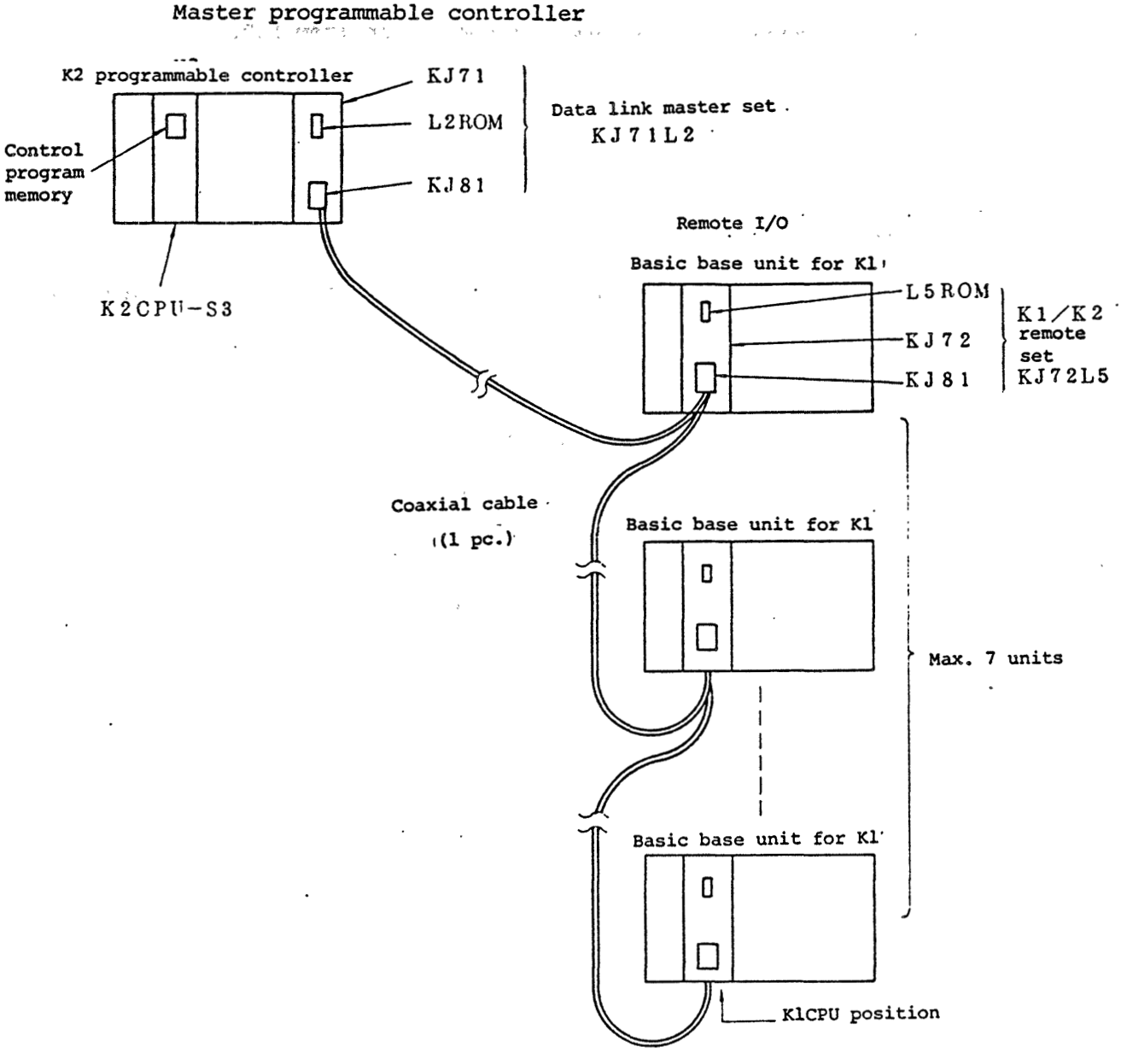


Fig. 5.8 Remote I/O system with K2CPU and K1, K2 I/O units

5.3.2. Specifications

(1) KJ72 is installed in the K1CPU position of the K1 base.

(2) The other specifications are the same as in item 5.2.

5.3.3. Program method

Same as for the remote I/O system with K2CPU and K0 unit (system 2) of item 5.2.

5.3.4. Caution items

Please note that the following units can not be used on the remote I/O side.

(1) KT61 timer unit

(2) KN61, KN62 external trouble monitor unit

(3) KA62, KA63, KA64, A/D, D/A conversion unit

(4) KD61 high-speed counter unit

(5) 8 point I/O mixed units like KH10 etc.

(6) Same input and output numbers for KH32

5.4. Dispersed control system by K2 and K0

5.4.1. Configuration

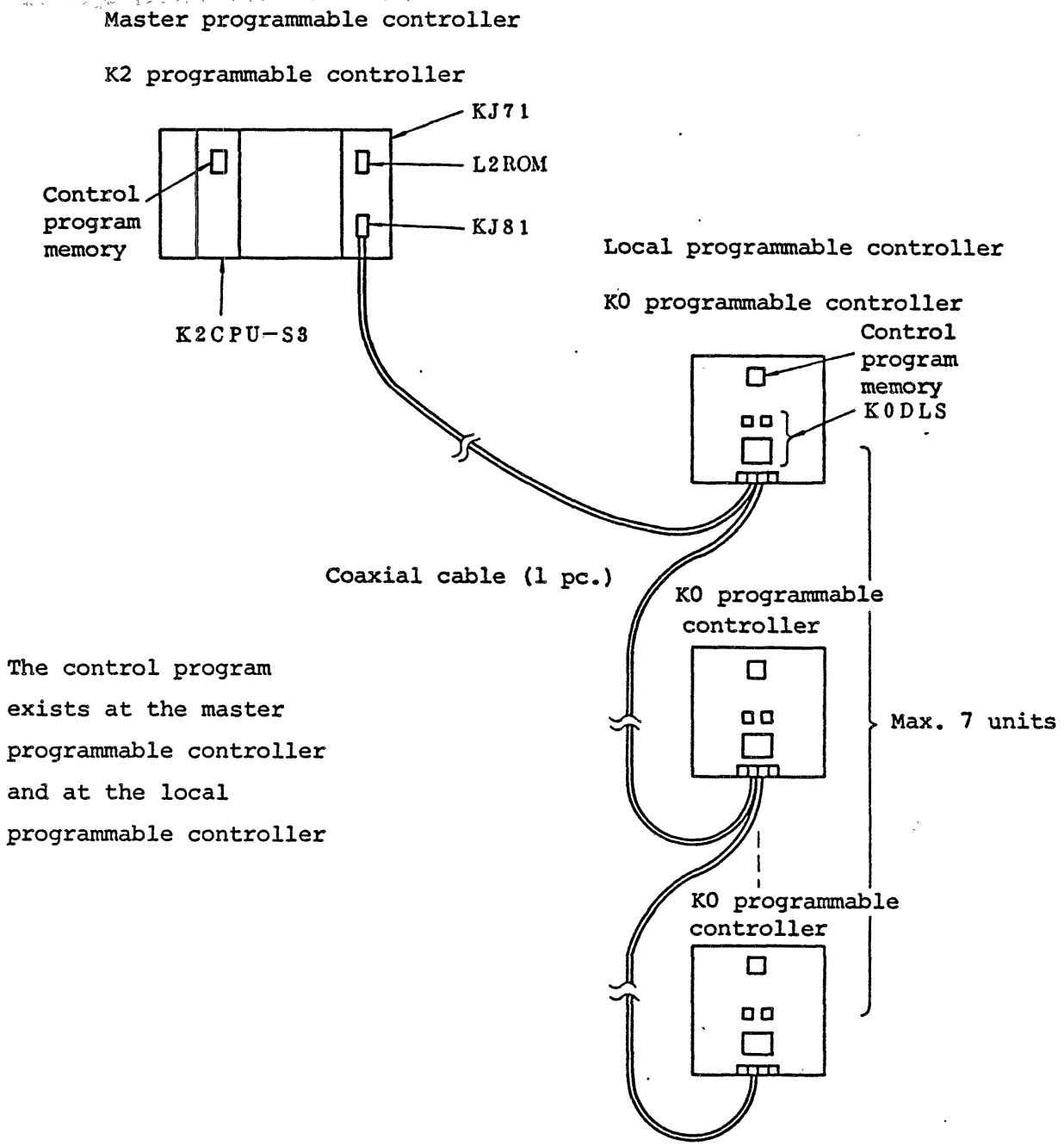


Fig. 5.9 Dispersed control system by K2 and K0

5.4.2. Specifications

(1) K2 programmable controller (master programmable controller) specifications

- o Number of I/O points: Max. 224 points (512 points (K2 points) - 256 points (link points) - 32 points (KJ71))
- o The other specifications are the same as for the K2 by itself.

(2) K0 programmable controller (local programmable controller) specifications

- o Except for addition of the data link set (K0DLS), the specifications are exactly the same as for the K0 programmable controller by itself.

(3) Total number of I/O points: 224 points + 128 points x 7 units = 1,120 points (max.)

(4) Transmission system specifications

- o The specifications are the same as for the remote I/O system with K2 and K0 of item 5.2.

(5) Data link point number (total)

- o Local to master
- o Master to local

} Total 256 points

Notes:

1) The above point number is the total number of points for transmission and reception between all local programmable controllers and the master programmable controller.
The K2 program designates how many points each local programmable controller uses. (Refer to item 5.4.3.)

2) Direct data links between the local programmable controllers are not possible. When such links are required, they must be executed via the main programmable controller.

3) Use of data registers other than the above point numbers for execution of large-capacity data links also is possible. (Refer to item 6.)

(6) KJ71 insertion position

o Insertion is possible in any I/O unit position of the K2 programmable controller, but insertion in the last position is recommended.

5.4.3. Program method

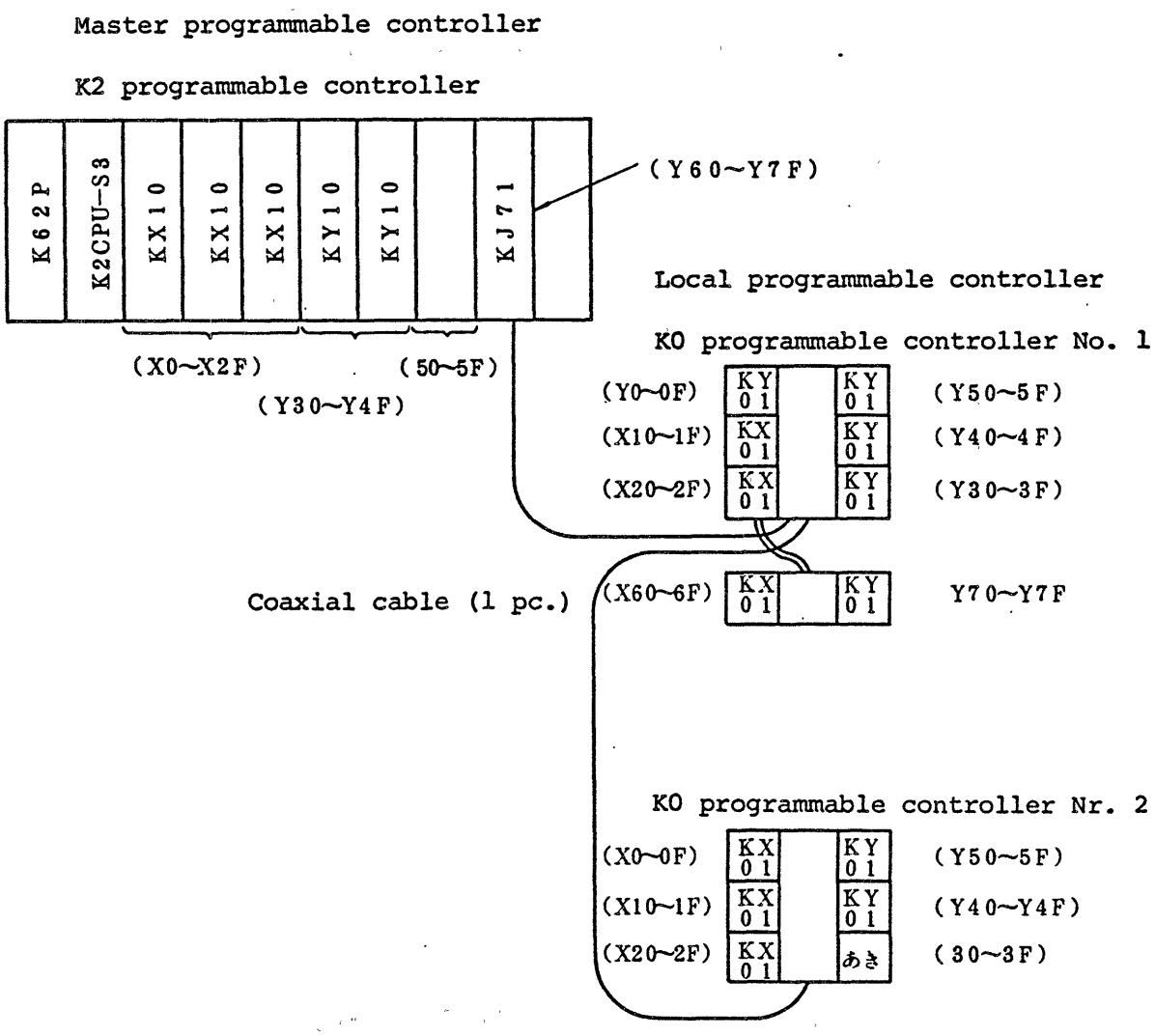


Fig. 5.10 Configuration example

(1) I/O numbers for each programmable controller

o The numbers in brackets in the above figure become the I/O numbers.

o The numbers are exactly the same as for use of the programmable controller by itself.

(2) Division of the data link area

o Division designation of the data link area to the individual local programmable controllers is designated by the program of the K2 programmable controller as shown in Fig. 5.11.

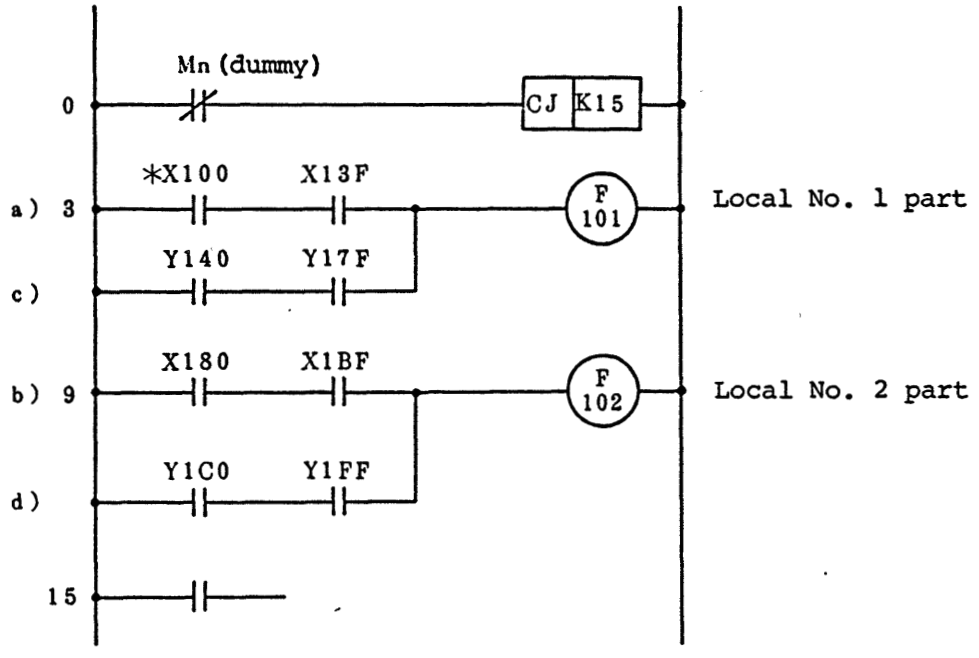


Fig. 5.11 Initial program

Notes:

1) In the example of the above figure, 128 points each of the max. 256 data link points are used for No. 1 and No. 2.

a) Local No. 1 → Master

Y100 to Y13F → X100 to X13F

b) Local No. 1 ← Master
X140 to X17F ← Y140 to Y17F

c) Local No. 2 → Master
Y180 to Y1BF → X180 to X1BF

d) Local No. 2 ← Master
X1C0 to X1FF ← Y1C0 to Y1FF

As shown in the above figure, the transmission side uses Y and the reception side uses X.
The numbers in the above figure designate the X and Y numbers on the master side.
The transmission side uses coil instructions (OUT, SET, etc.), and the transmission side uses contact instructions (LD, OR, AND, etc.).
The above figure has the same format as item 5.2.3.(2), but it should be noted that the leading I/O numbers at the * link positions must be from 100 on.

(3) Program method (master programmable controller)

Start the program after the initial program of Fig. 5.11.
The program method is the same as for the K2 by itself.

Program example for a distributed control system

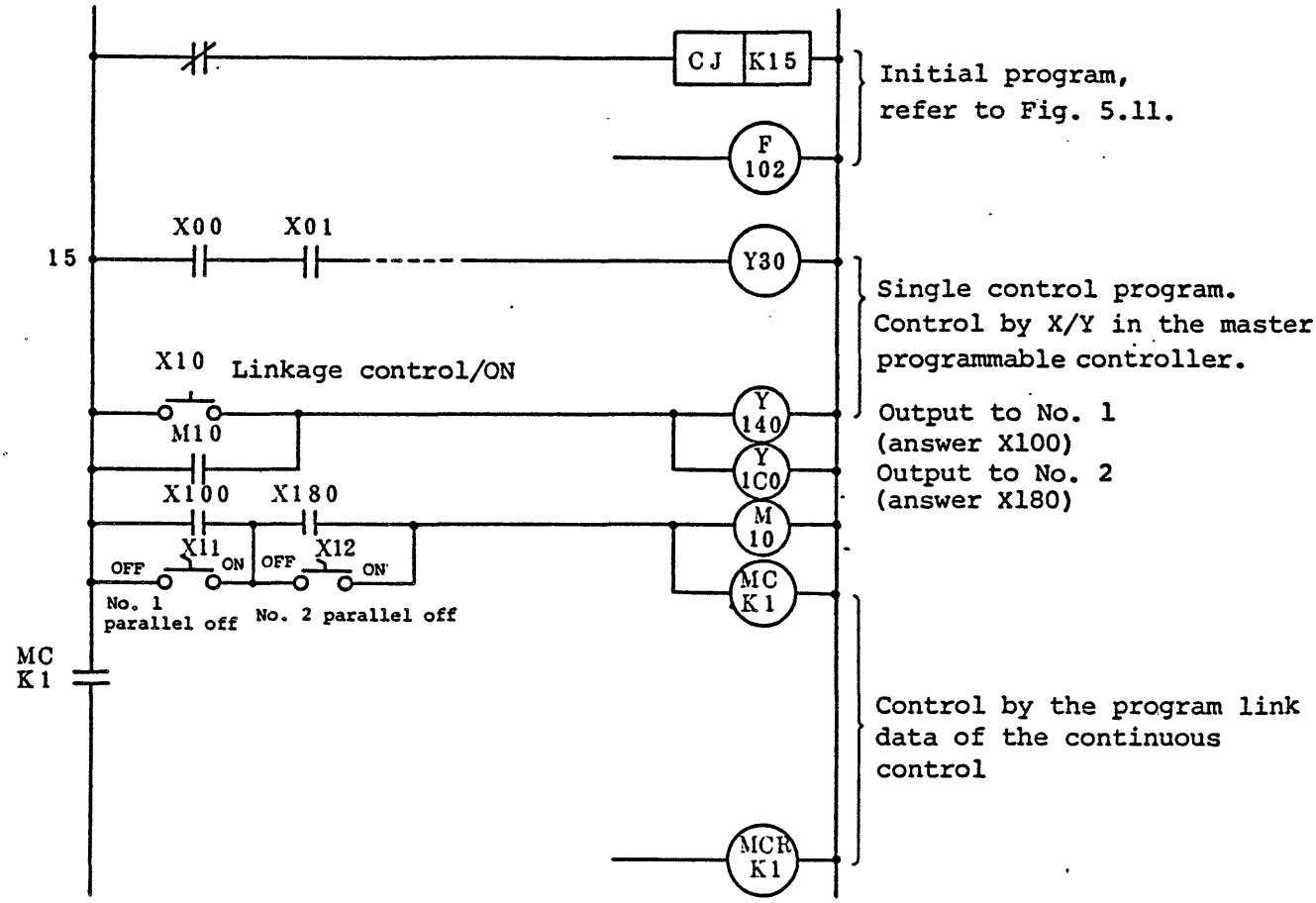


Fig. 5.12 Master programmable controller program

Local programmable controller Nr. 1

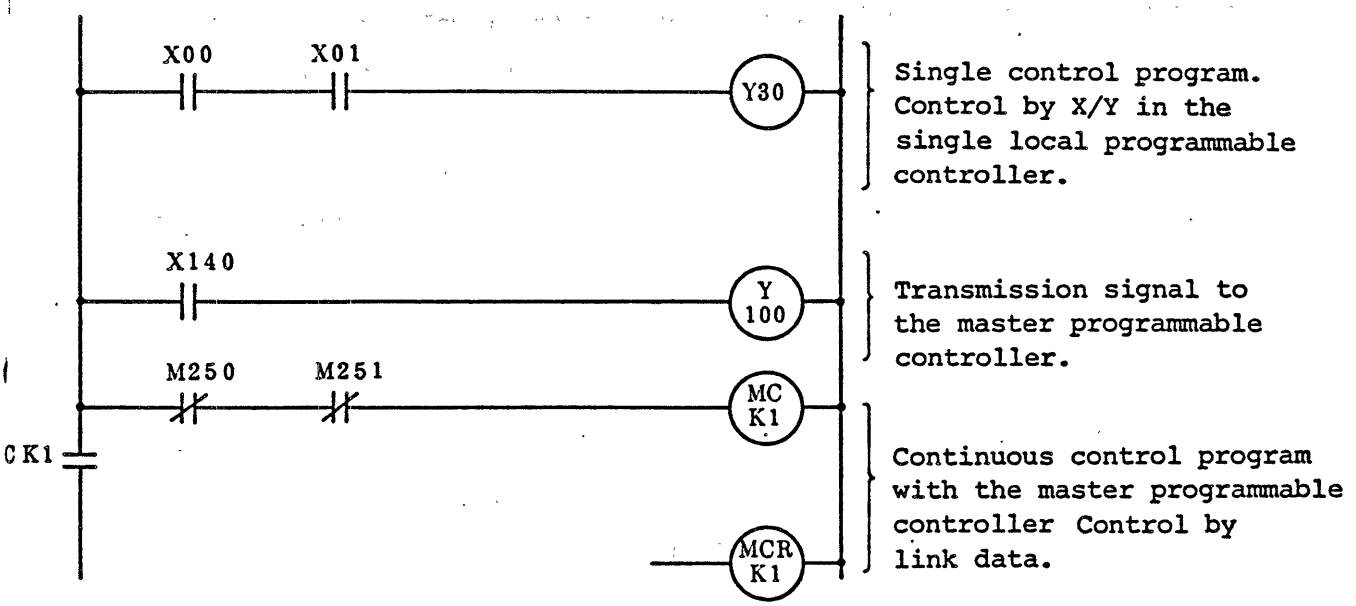


Fig. 5.13 Local programmable controller Nr. 1 program

Local programmable controller Nr. 2

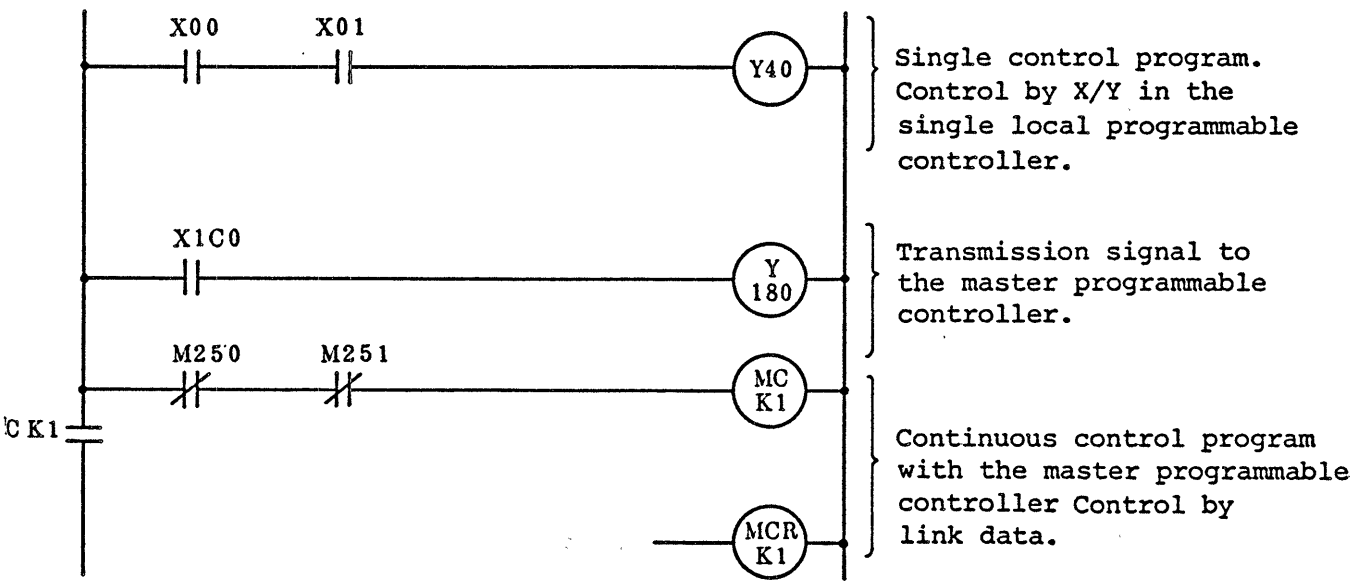
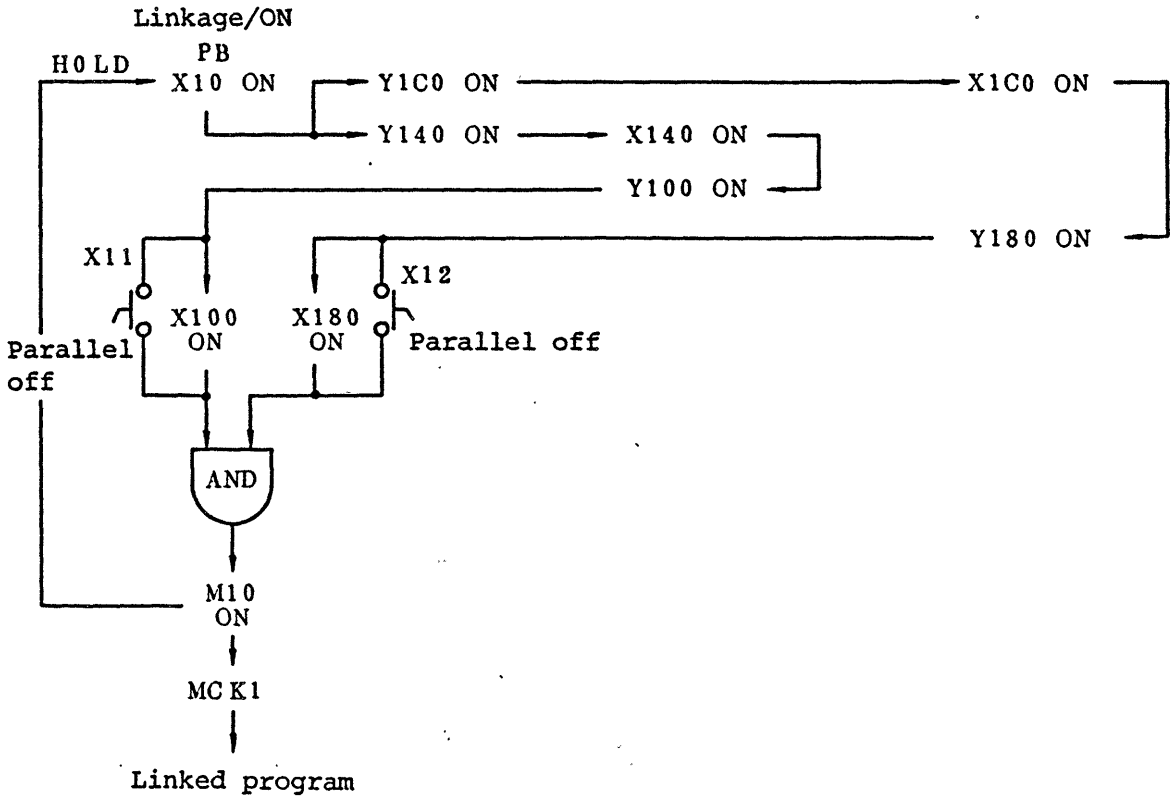


Fig. 5.14 Local programmable controller Nr. 2 program

The control programs (individual control) by the input and output units for the master programmable controller and the local programmable controllers are exactly the same as the conventional programs, and there are no limitation items. However, the linked control (dispersed control) program by the link data shown in Fig. 5.12 to Fig. 5.14 must have interlock conditions inserted by master control instructions to be fail-safe.



When for example the local programmable controller No. 1 comes down, Y100 becomes OFF, MCK1 of the master programmable controller becomes OFF because of linkage with the master programmable controller, and the linked program is interrupted.

For parallel off operation with No. 1 in down condition, for example the selector switch for the parallel off signal X11 should be installed on the process input on the side of the master programmable controller, X100 should be bypassed by this, and then linked operation again should be executed by setting linkage/ON X10 again to ON.
On the other hand, when the master programmable controller becomes down, the data link is interrupted, M251 becomes ON, and the linkage control program (Fig. 5.13) becomes OFF by MCK1.
However, as the individual control program is programmed at a position excluded from MCK1, individual operation is possible.

5.4.4. Hardware setting for master programmable controller and local programmable controllers

(1) Master programmable controller

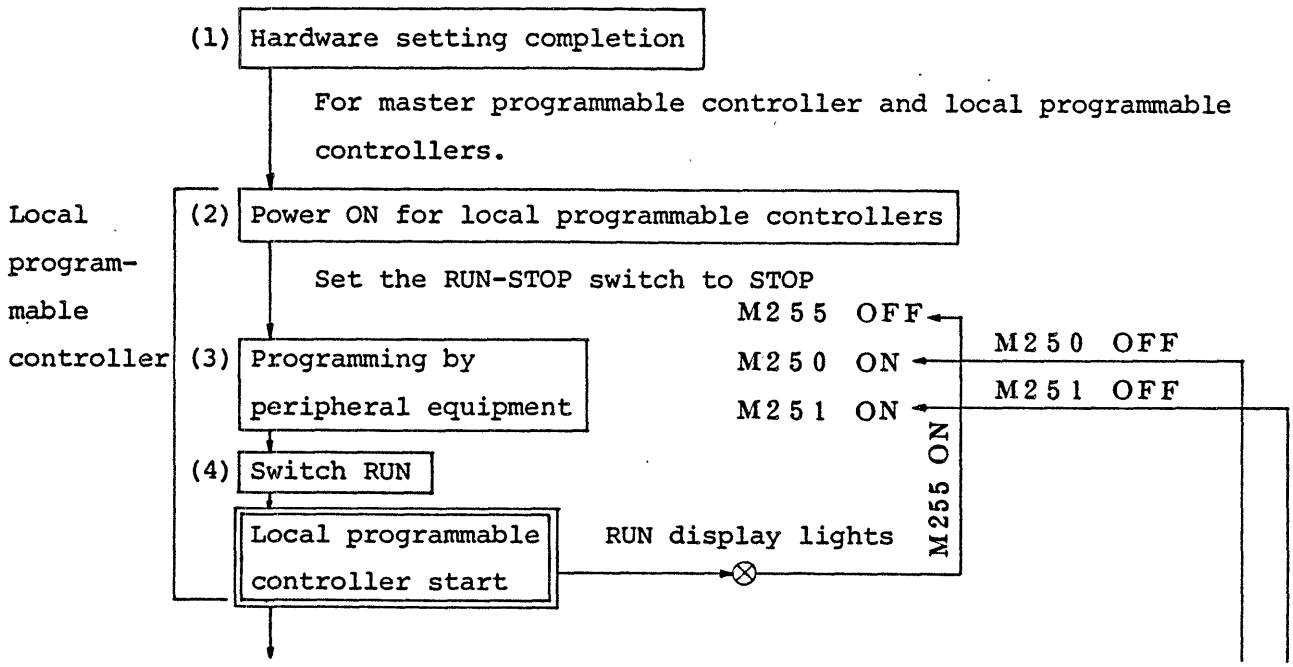
Same as for item 5.2.4.(1).

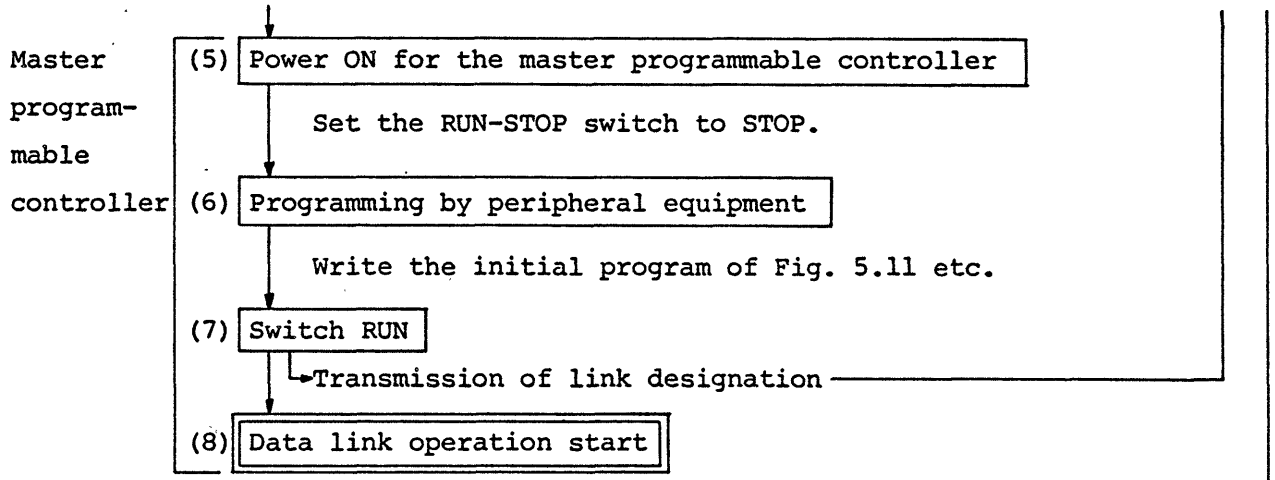
(2) Local programmable controllers

The setting is the same as for item 5.2.4.(2), but switch selection is to be executed according to table 4.4.

5.4.5. Operation sequence

(1) Operation start





Note:

The power ON sequence principally should be started with the remote I/O stations and then should proceed to the master programmable controller. (When the programming for the master programmable controller has been completed, simultaneous power ON also is possible.)

(2) Operation stop

Execute operation stop basically in the reverse order of operation start. When the RUN-STOP switch of the master programmable controller is set to STOP, the master programmable controller will stop, and as transmission and reception will be interrupted, M251 of the local programmable controllers will become ON, and as shown in the program of Fig. 5.13, the linked control program becomes OFF by MCK1. (However, the individual control program continues.)
Operation restart will be executed when the RUN-STOP switch of the master programmable controller again is set to RUN.

(3) Remote I/O station parallel off

Parallel off operation for the local programmable controllers is possible. By setting the RUN-STOP switch of the local programmable controller No. 1 to STOP as shown in the program of Fig. 5.12, all Y signals to the master programmable controller (X as seen from the master programmable controller) become OFF and the data link is continued, so that MC K1 becomes OFF and the linked control program is interrupted immediately. For this reason, parallel off can be executed without linked control program interruption by executing STOP for the local programmable controller after switching the No. 1 parallel off signal (X11), prepared in advance by process input, to OFF. For cancellation of parallel off, set the local programmable controller to RUN, and then set the parallel off signal (X11) to OFF. Then the original fail-safe circuit again will become effective.

5.4.6. Trouble contents and treatment

These are the same as for item 5.2.6., but reference should be made to table 5.1.

5.5. Dispersed control system by K2 and K2

5.5.1. Configuration

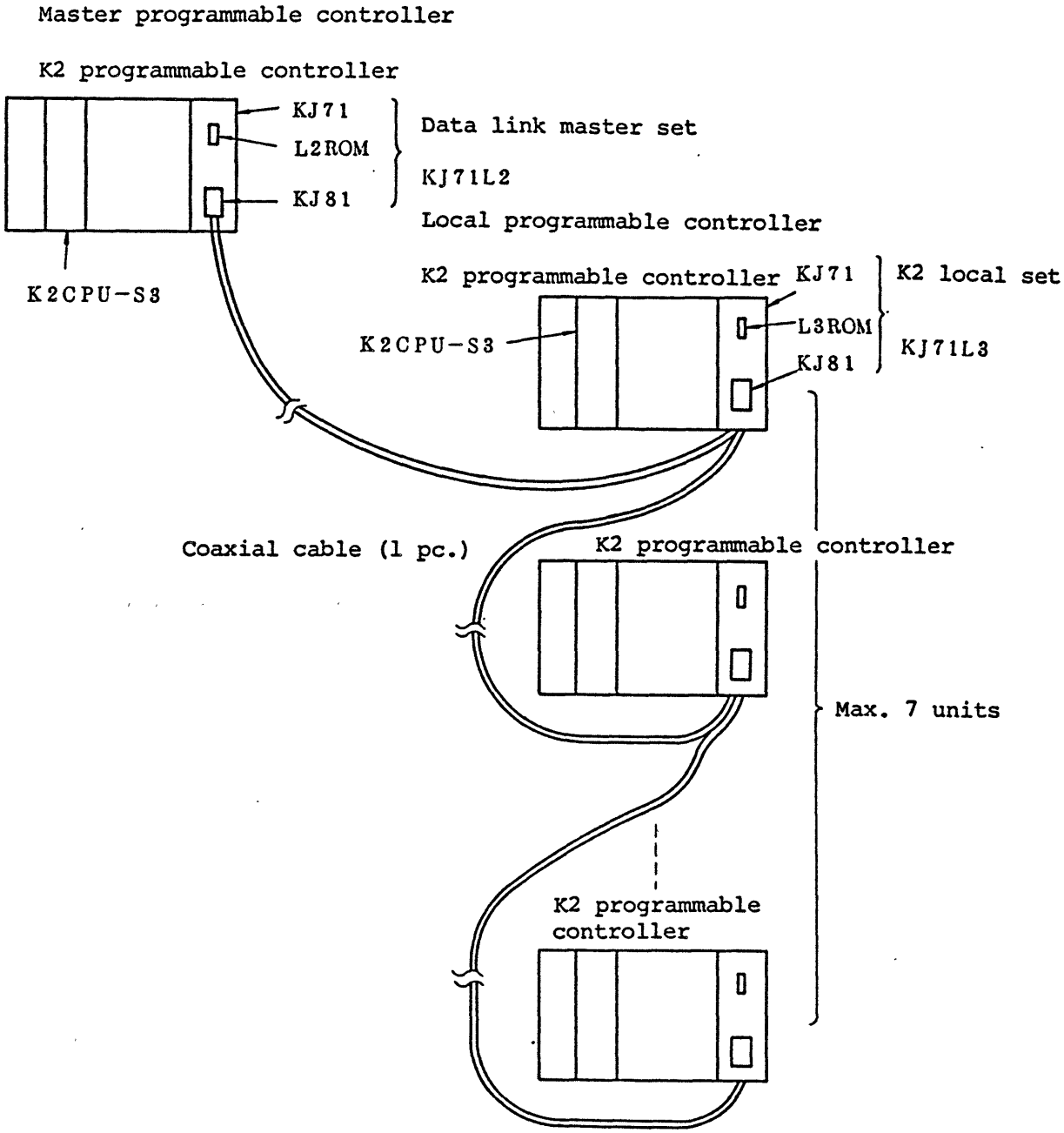


Fig. 5.15 Dispersed control system by K2 and K2

5.5.2. Specifications

(1) K2 programmable controller (master and local) specifications

o Number of I/O points: Max. 224 points

o The other specifications are the same as for the individual K2.

(2) Total number of I/O points: Max. 224 x 8 = 1,792 points

(3) The other specifications are the same as for item 5.3.2.

Note: The program method also is the same as for item 5.3.3.

5.5.3. Program method

Same as item 5.3.3., so refer to item 5.3.3.

5.5.4. Hardware setting for master programmable controller and local programmable controller

Refer to item 5.2.4.

5.5.5. Operation sequence

Refer to item 5.2.5.

5.5.6. Trouble contents and treatment

Refer to item 5.2.6.

5.6. Computer link system

5.6.1. Outline

This is the computer link unit using a series data link unit (KJ71) and an RS-232C adapter (KJ82) for data exchange between a programmable controller (K2CPU-3S) and a computer, for example a personal computer. The purpose of this link unit is monitoring of the operation status of the programmable controller on the computer side as well as reading and rewriting of the contents of programmable controller data registers etc., and reading is possible for all X, Y, M, T, C, F, and D of the programmable controller, while writing is possible for Y, M, T, C, F, and D. However, program reading and writing is not possible.

5.6.2. Computer link unit configuration

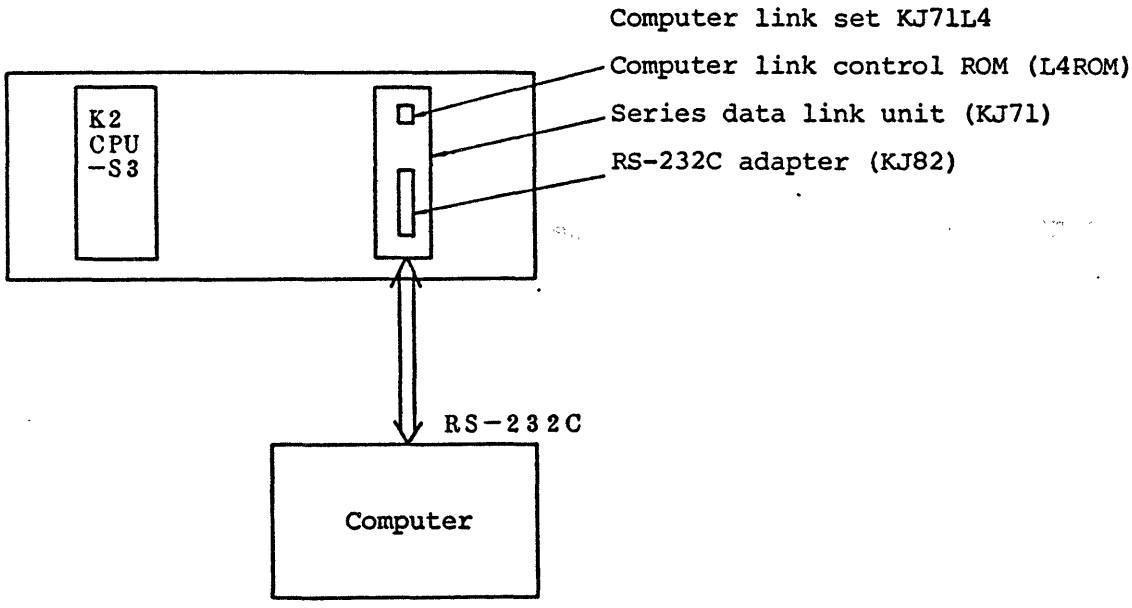


Fig. 5.16 Computer link unit configuration

(1) KJ71 can be installed in any I/O slot of the base unit for K2.

(2) The RS-232C adapter (KJ82) and the computer link control ROM (L4ROM) are installed on the KJ71.

Note:

The external interface specifications are decided by the KJ71 control program, and the L4ROM control specifications are as follows.

5.6.3. Transmission specifications

(1) Transmission method: Start-stop synchronization method

(2) Transmission speed: 1200, 2400, 4800, 9600 BPS (selectable)

(3) Data format

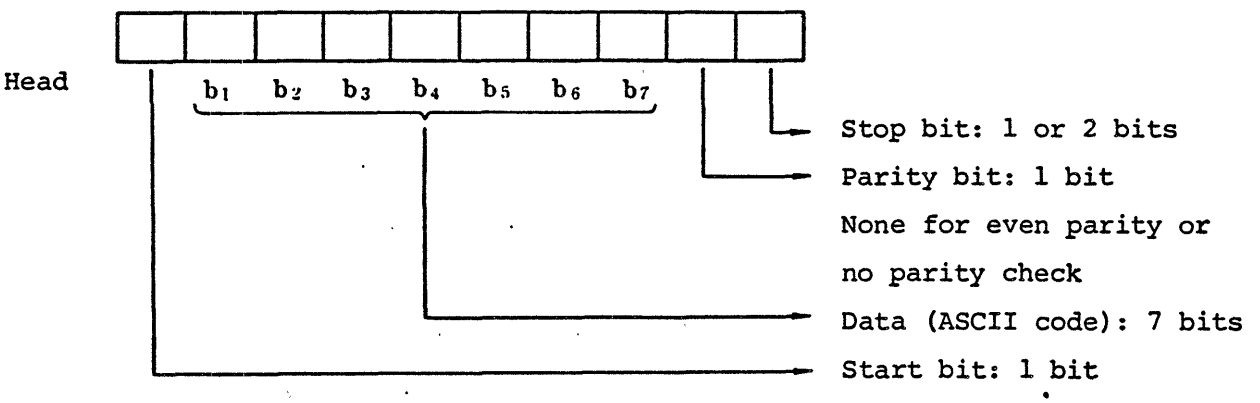


Fig. 5.17 Data format

(4) Designation of the transmission specifications

(i) Designation with switches in KJ71

Table 5.2 Switch designation in KJ71

Switch No.	At the time of OFF	At the time of ON
1	1200/2400 BPS (note 1)	4800/9600 BPS (note 2)
2	No parity check	Parity check
3	No sum check	Sum check
4	Writing during RUN of the programmable controller possible	Writing during RUN of the programmable controller impossible
5	Stop bit: 1 bit	Stop bit: 2 bits
6	The switches 6 to 8 must be set to OFF.	
7		
8		

Note 1: Designation of 1200 or 2400 BPS is made with the KJ82 selection chip.

Note 2: Designation of 4800 or 9600 BPS is made with the KJ82 selection chip.

(ii) Designation by the KJ82 selection chip (switching by CON3)

- o Set chip 3 to ON for generation of the reception clock in KJ82, and set chip 4 to ON for generation of the transmission clock in KJ82. Set the respective chips to OFF for external clock use.
- o For 2400 or 9600 BPS: Chip 1 OFF, chip 2 ON (insertion)
- o For 1200 or 4800 BPS: Chip 2 OFF, chip 1 ON (insertion)

5.6.4. Hardware specifications

o The hardware specifications are according to EIA RS-232C.

(1) Recommended connection method

KJ71 side			Cable connection and signal direction	Computer side	
Terminal name (note 4)		Terminal No.		D-SUB pin No.	Signal name
	FG2	TB11	→	1	FG
(RXD)	TXD2	TB12	→	2	TXD
(TXD)	RXD2	TB13	→	3	RXD
(CTS)	RTS2	TB14	→	4	RTS
(RTS)	CTS2	TB15	→	5	CTS
(DTR)	DSR2	TB16	→	6	DSR
	SG2	TB17	→	7	SG
			→	8	CD
			→	15	TXC
			→	17	RXC
(DSR)	DTR2	TB20	→	20	DTR

Note 1: Connect the shield of the connection cable to the KJ71 terminal (FG2).

Note 2: KJ71 output

(1) RTS becomes ON by hardware ready status on the KJ71 side.

(2) DTR becomes ON by data reception possible status on the KJ71 side.

Note 3: KJ71 input (processing by DSR)
Transmission sequence initializing by DSR OFF.

* DTR and DSR must be connected so that they are ON during transmission from the computer side.

Note 4: The KJ71 terminals are shown matched to the signal names from the computer side. Accordingly, they correspond to the signals in brackets inside the KJ71.
KJ71 has 2 channels, and channel 2 is used as shown above.

5.6.5. Transmission control sequence (protocol)

Transmission start must be applied from the computer side. Transmission start from the KJ71 side is not possible.

(1) Sequence data reading sequence

This is the sequence for reading the data of the programmable controller on the computer side.

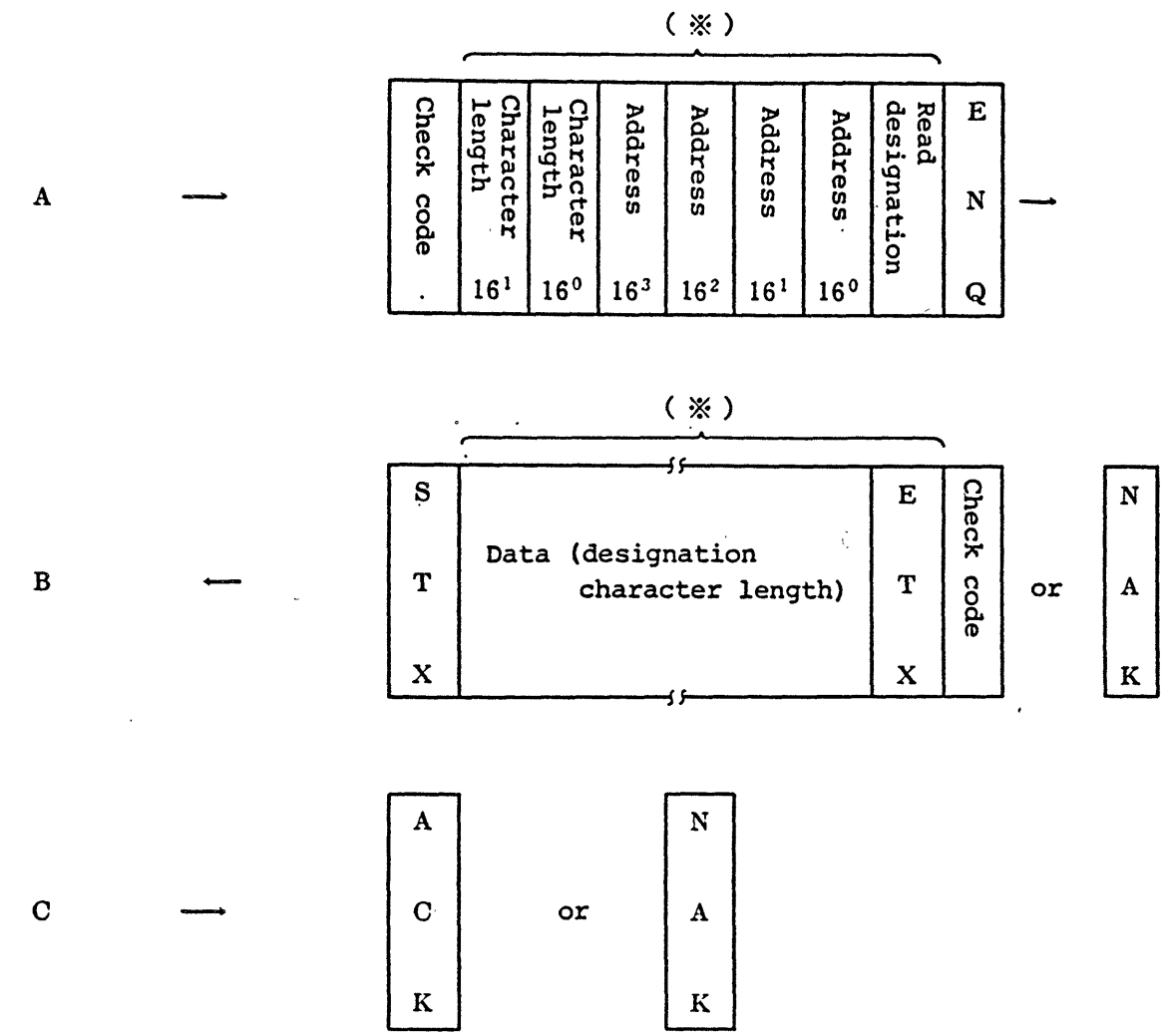


Fig. 5.18 Sequence for reading of the data of the programmable controller

(2) Sequence for writing data into the programmable controller

This is the sequence for writing data into the programmable controller from the computer side.

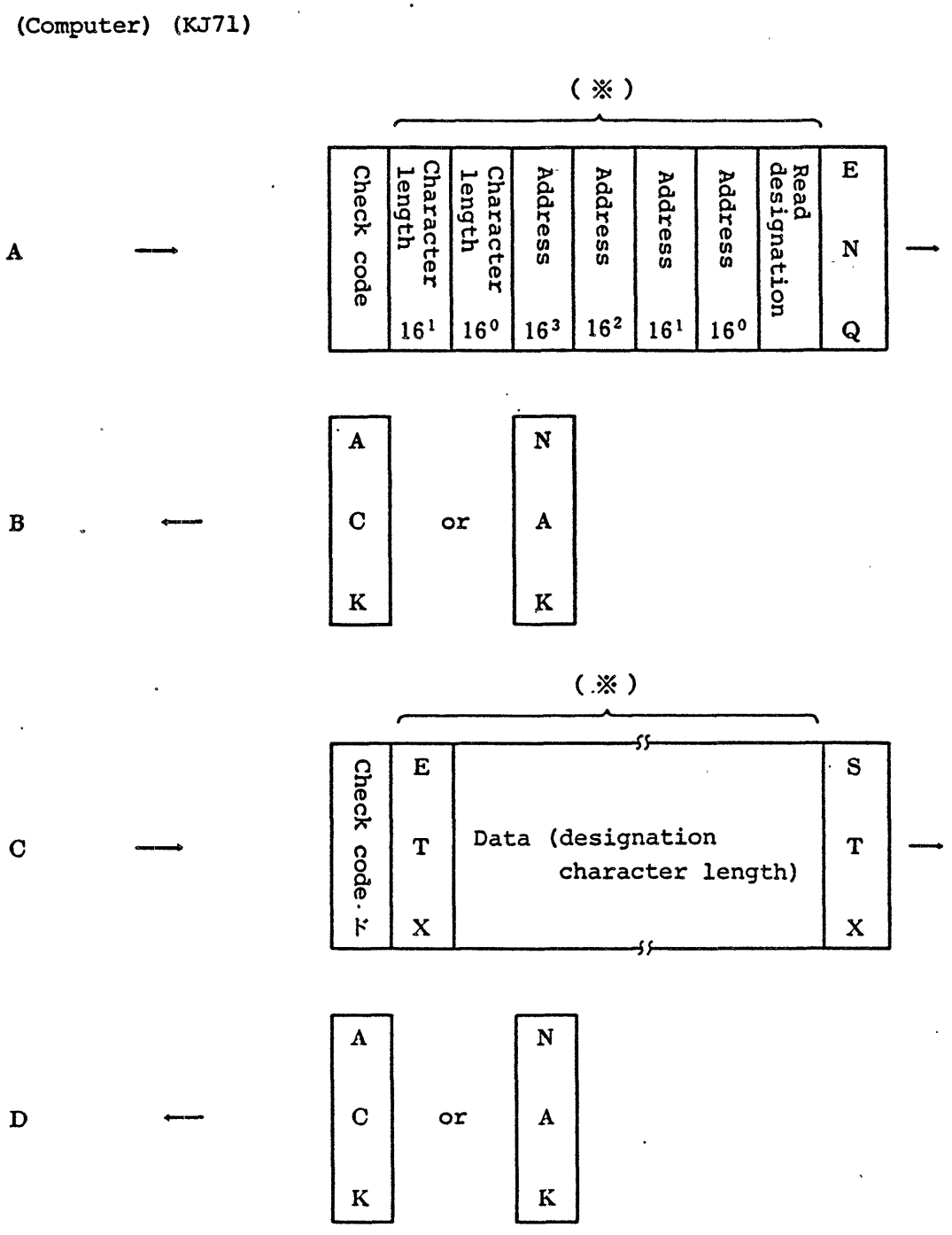


Fig. 5.19 Sequence for writing of data into the programmable controller

Note 1: The sum check code is used as check code, and it is applied in regard to the character of (*). However, this is not required when sum check off is specified in 3-(4).

Note 2: The transmission codes are as follows.

- o ENQ: 05H (H designates hexadecimal numbers)
- o STX: 02H
- o ETX: 03H
- o ACK: 06H
- o NAK: 15H
- o Write designation: 11H
- o Read designation: 12H

Note 3: When the KJ71 side does not respond with the normal sequence, initialize the KJ71 transmission sequence with the following code.

- o EOT: 04H or CL:0CH

The transmission sequence on the KJ71 side is initialized after transmission of NAK or at the time of reception of NAK.
The transmission sequence naturally also is initialized at the time of completion of the normal transmission and reception signal according to 5.6.5.(1) and 5.6.5.(2).

Note 4: The addresses are the sequence-internal addresses listed in item 5.6.6.
Accordingly, convert the 4 digit hexadecimal numbers according to the ASCII code as shown below for transmission.

Example: For the sequence-internal address 71F0H

- Address 16^0: 0 becomes 30H
- Address 16^1: F becomes 46H
- Address 16^2: 1 becomes 31H
- Address 16^3: 7 becomes 37H

Hexadecimal numbers ASCII code

Note 5: The character length is the character length of the read/write data, and it is 2 digits of hexadecimal numbers (max. 255). Transmit after conversion according to the ASCII code in the same way as for the addresses.

Example: For the character length 1E (hexadecimal number)

{ Character length 16^0: E becomes 45H
{ Character length 16^1: 1 becomes 31H

Hexadecimal numbers ASCII code

Note 6: Transmit read/write data also after conversion of 1 byte (2 digit hexadecimal number) according to the ASCII code.

1 byte data 12H
16^0: 2 becomes 32H
16^1: 1 becomes 31H

ASCII code

Note 7: Data processing at the time of read/write is executed byte by byte in regard to the K2CPU-S3.
Accordingly, when present values of timers and other data requiring 2 bytes are read, care is required as the following will occur.

Example:

o Reading of the present value of T0

The present value of T0 is arranged as

7100#	(L)
7101#	(H)

When now the read command from the computer comes at the time when the present value is

7100#	FF
7101#	00

, FF# will be read first as the address 7100. Next, reading of the address 7101# is difficult, as it shall be assumed that the timer instruction has been executed before this reading. Then the present

7100#	00
7101#	01

value becomes , and when now the address 7101# is read, the data 01# will be read and the result becomes

FF
01

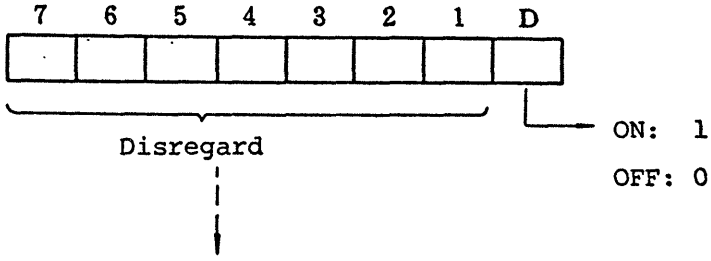
.

This means that the correct data are not obtained. Accordingly, countermeasures like reading twice and using the data only in case of coincidence etc. are required.

5.6.6. Addresses in the programmable controller

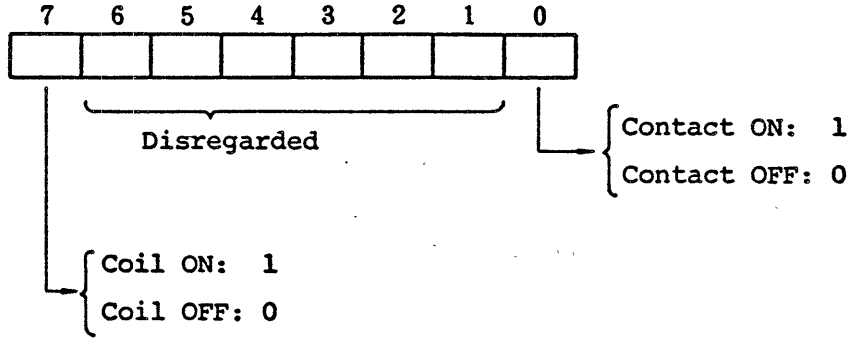
(1) Process input: X0 to X1FF	6800H to 69FFH (*1)
(2) Process output: Y0 to Y1FF	
For writing:	6800H to 69FFH (*1)
For reading:	6400H to 65FFH (*1)
(3) Temporary storage: M0 to M255	7000H to 70FFH (*1)
(4) TC present value: T.C0 to T.C127	7100H to 71FFH (*3)
(5) TC contact, coil:	7400H to 747FH (*2)
(6) Data register: D0 to D127	7200H to 72FFH (*3)
(7) External trouble monitor: F0 to F127	7300H to 737FH (*1)
(8) Master control K0 to K63	7500H to 753FH (*1)

Note 1: As only the lowest bit of one byte is effective for (*1), the others should be masked.



(Disregarded on the side of the programmable controller. Masking should be executed on the side of the controller.)

Note 2: Only the top bit and the bottom bit are effective for (*2).



Note 3: (*3) are 2 byte data.

	7 6 5 4	3 2 1 D
Lower digit	16^1	16^0
Upper digit	16^3	16^2

o For the above addresses, reading and writing can be executed any time even during RUN of the programmable controller, but sufficient attention should be paid to safety.
(When writing during RUN is not to be executed, it is safer to set the SW4 of table 5.2 to ON.)

5.7. In regard to expansion of the number of I/O points

For the dispersed control systems of item 5.4 and item 5.5, the max. number of I/O points for the K2 programmable controller has been stated as 224 points, but this is only recommended for easily understandable programming with 100 to 1FF as the data link I/O numbers.
Accordingly, the number of I/O points of the K2 programmable controller can be increased further when the number of data link points is reduced.

Example: Use of X180 to 1BF and Y1C0 to 1FF for linkage

The max. number of I/O points for the K2 programmable controller becomes 352 points (224 points + 128 points).

6. Data link method for the dispersed control system

For the dispersed control system by K2/K0 of item 5.4 and the dispersed control system by K2/K2 of item 5.5, data linkage for a total of 256 points is possible between master programmable controller and local programmable controllers, and this chapter explains how linkage for a larger data volume can be executed by use of data registers and function instructions F120 to F124.

6.1. Special registers for data linkage

(1) D120: For designation of the local programmable controller number (station number)

(2) D121: For designation of the leading register number of the reception and transmission register (D0 to D95)

(3) D122: For designation of the reception and transmission register length

Example:

Execution of data communication with use of the local programmable controller No. 2 and D10 to D29

o D120 ← 2: No. 2

o D121 ← 10: D10 is the start

o D122 ← 20: 20 pcs. from D10 to D29

6.2. Data link function instructions

(1) F120: Write instruction on the M (master) side for transmission data from M to L (local)

(2) F121: Read instruction on the L side for transmission data from M to L.

(3) F122: Data transmission request instruction from M in regard to L.

(4) F123: Write instruction on the L side for transmission data from L to M.

(5) F124: Read instruction on the L side for transmission data from L to M.

Note: The initiative for data transmission and reception between M and L is on the M side. Accordingly, (4) F123 is executed when the transmission request of (3) has been received.

6.3. Program method for data transmission from the master programmable controller to the local programmable controller

6.3.1. Program on the M (master) side

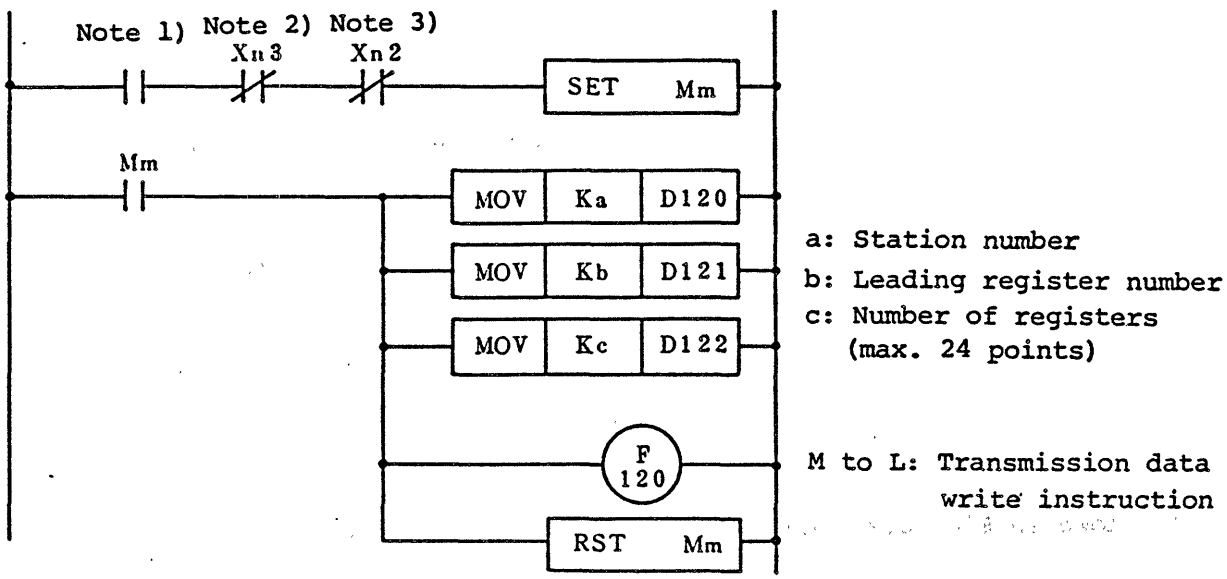


Fig. 6.1 Program on the master side

6.3.2. Program on the local (L) side

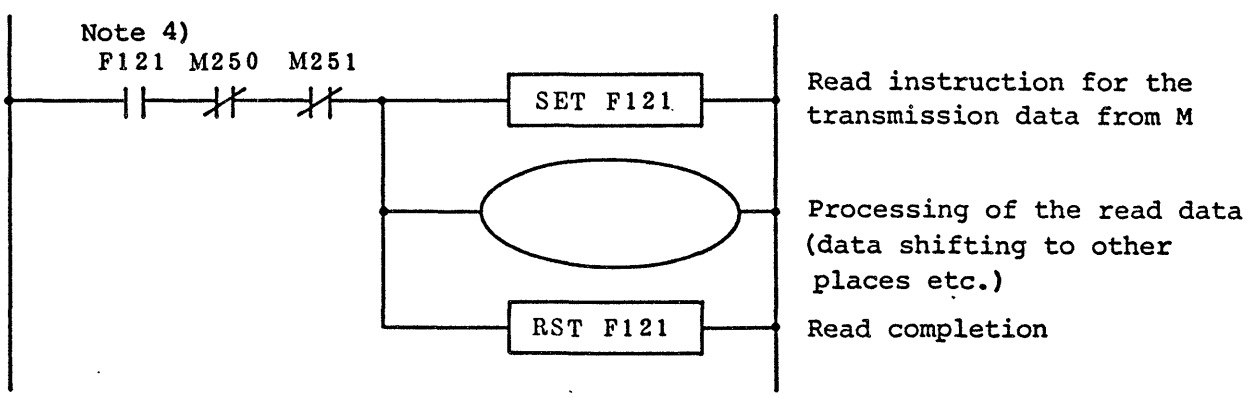


Fig. 6.2 Program on the local side

Notes:

1) Start signal for transmission from M to L.

2) Xn3: During data reception from L to M. Transmission is

3) Xn2: During data transmission from M to L. interlocked.

4) This is the contact indicating that data have been transmitted from M to L.

5) n: KJ71 installation slot number (example: "0" when the KJ71 is installed next to the CPU in the basic base.)

6) m: Any number from M0 to M249

7) Naturally, the data to be transmitted have to be set in advance into Db to (Db + c - 1).

8) Data register transmission has max. 24 points. Accordingly, KC may not exceed 24. Also, as D95 is the maximum for the data register, (b + C - 1) must be within 95.

9) The programs of Fig. 6.1 and Fig. 6.2 are to be used inserted before the last END instruction on master and local side.

10) As shown in Fig. 6.2, the B contact for M250 (designation for initial information existing = OFF) and M251 (communication normal = OFF) must be inserted on the local side.

6.4. Program method for data transmission from local to master programmable controller

Data transmission from local to master is executed on receipt of a data transmission request from the master side.

Arbitrary data transmission from local to master is not possible.

6.4.1. Program on the master (M) side

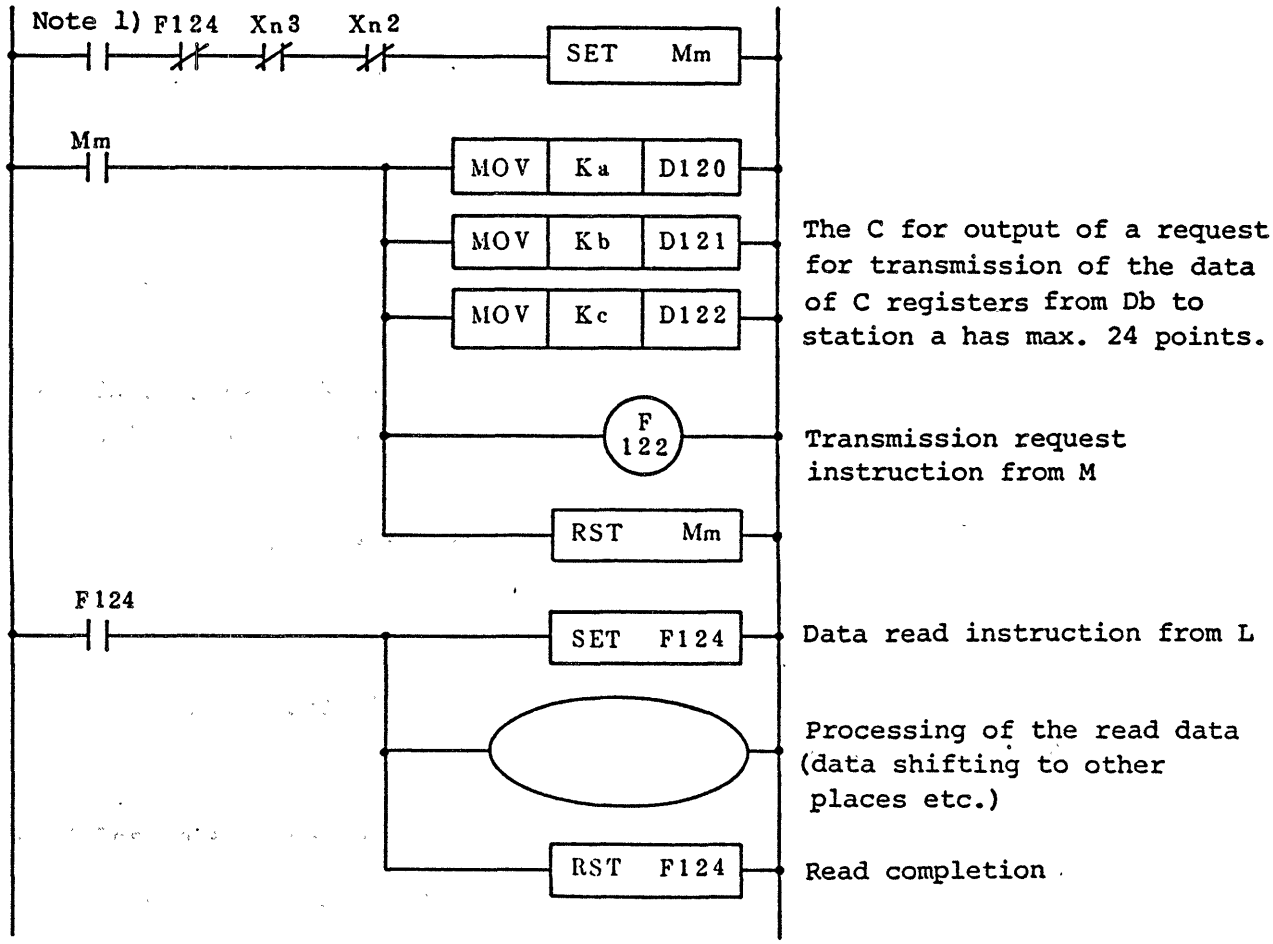


Fig. 6.3 Program on the master side

6.4.2. Program on the local (L) side

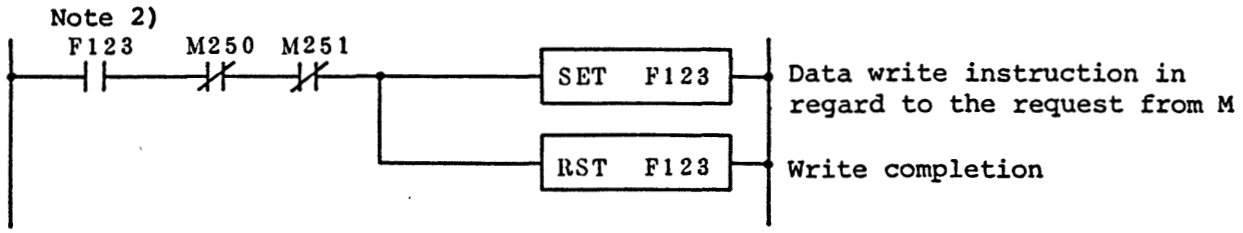


Fig. 6.4 Program on the local side

Notes:

1) Data request start contact to local

2) Contact indicating existence of a data transmission request from the master.

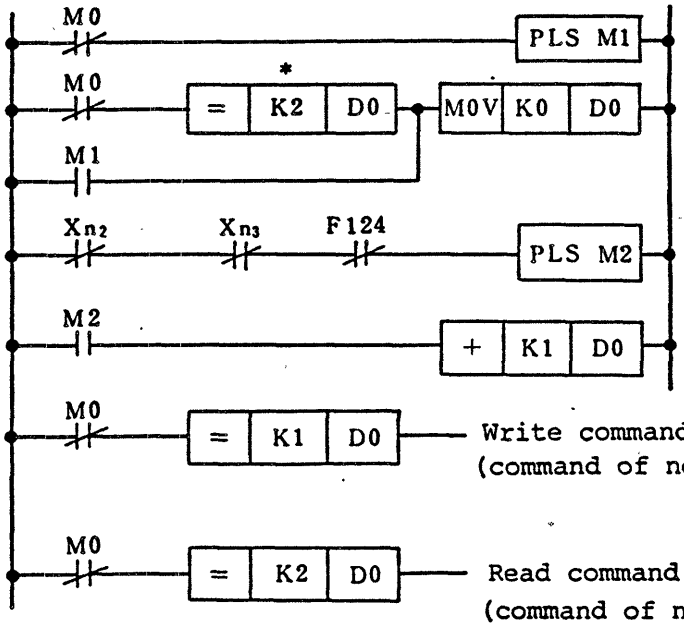
3) Data register transmission has max. 24 points. Accordingly, KC may not exceed 24. Also, as D95 is the maximum for the data register, (b + c - 1) must be within 95.

4) The programs of Fig. 6.1 and Fig. 6.2 are to be used inserted before the last END instruction on master and local side.

5) As shown in Fig. 6.2, the B contact for M250 (designation for initial information existing = OFF) and M251 (communication normal = OFF) must be inserted on the local side.

6.5. Method for repeated continuous data transmission between master and local

This is a program example for alternate repeated continuous data transmission (write) from master to local and data transmission (read) from local to master.



D0 = 0 at the time of initializing.
D0 = 0 for D0 = 3.

Add 1 to D0 at the time of read and write completion.

Write command
(command of note 1 of Fig. 6.1)

Read command
(command of note 1 of Fig. 6.3)

M0 is a dummy contact, D0 = 0 exists at the time of D0 initializing and at the time of D0 = 3, 1 is added to D0 at the time of read completion, a write request is issued at the time of D0 = 1, and a read request is issued at the time of D0 = 2. For continuous operation with 1:2 stations, use K = 5 for *, and execute a write request for station No. 2 for D0 = 3 and a read request for station No. 2 for F0 = 4.

7. Application examples for data link systems

(1) Mixed use of remote I/O by K2CPU and K0 unit (system 2), dispersed control system (system 4), and K2CPU dispersed system (system 5) is possible.

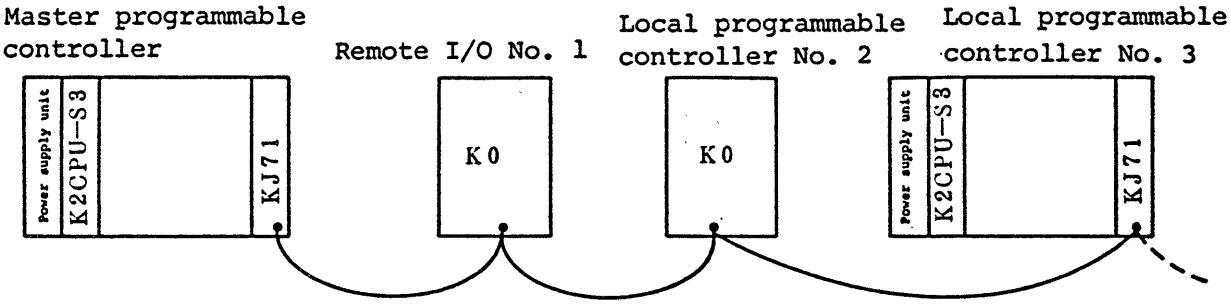


Fig. 7.1 Mixed remote and local system

In regard to the programming handling, refer to items 5.2., 5.3., 5.4., and 5.5.

(2) The systems 2 to 5 can be used for the individual programmable controllers of the K2CPU parallel data link system (system 1).

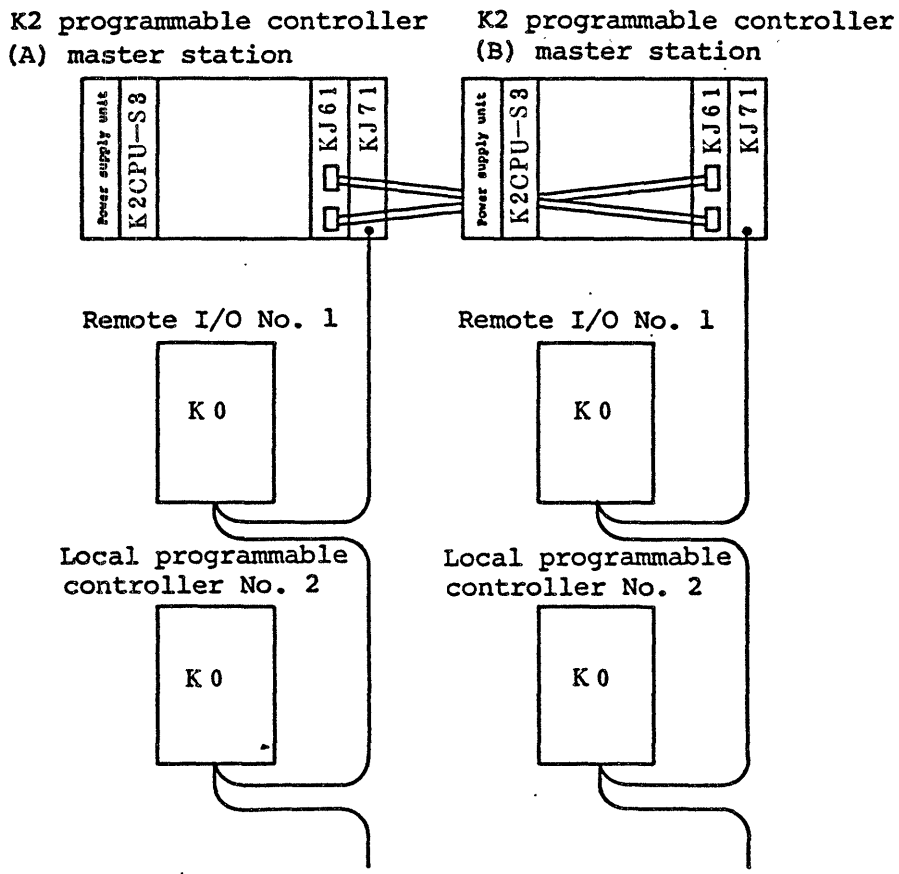


Fig. 7.2 Mixed system with parallel data link and remote, local

(3) Computer link system

The computer link system can be used installed on the basic (or extension) base of the K2CPU of the master programmable controller or the local programmable controller. However, care is required as only two KJ71 units can be installed on the basic base (the base on which the K2CPU is installed) because of the 5 V power supply capacity of the power supply unit (K61P/K62P).

8. Caution items for external wiring

8.1. Data link cable specifications and execution method

(1) Use the following type of coaxial cable for the systems 2 to 5.

Type name: Coaxial cable, high-frequency coaxial cable JISC3501
3C-2V or 5C-2V

(2) Cable length: Max. 500 m

Execute wiring sequentially from the master station to the remote (local) stations, and do not execute wiring with several wires at one receptacle.
The max. length for the sequential wiring is 500 m.

(3) Cable wiring route

As sufficient noise countermeasures have been executed, no special considerations for separation from other wires are required. However, wiring should be executed separated from power lines as far as possible.

8.2. Safety design and system operation sequence

Safety design may not be forgotten for design of a dispersed system. For example, sufficient care must be taken that the local programmable controller in a master/local system will not operate by itself when there is trouble for the master programmable controller.
On the other hand, there are also cases where it is desired to operate the local programmable controller as a temporary measure when there is trouble for the master programmable controller.
This link system has been designed as follows under sufficient consideration of the above items.

8.2.1. Programmable controller trouble detection and program method

(1) The data register (D124) of the master programmable controller can be used to find which remote station has trouble.

(2) The user can use D124 to establish a program to stop the entire system or a program permitting temporary operation with parallel off for the trouble station etc.

(3) The temporary storage of M250 and M251 on the local programmable controller can be used to establish a program for stop of the local station or for operation of the local programmable controller by itself etc.

M250: OFF when data communication with the master station is established.

M251: ON when communication trouble is detected on the local station side.

8.2.2. System operation sequence

The power ON sequence for the individual programmable controllers of the system is as follows.

(1) Execute power ON first for all local programmable controllers and finally for the master programmable controller.

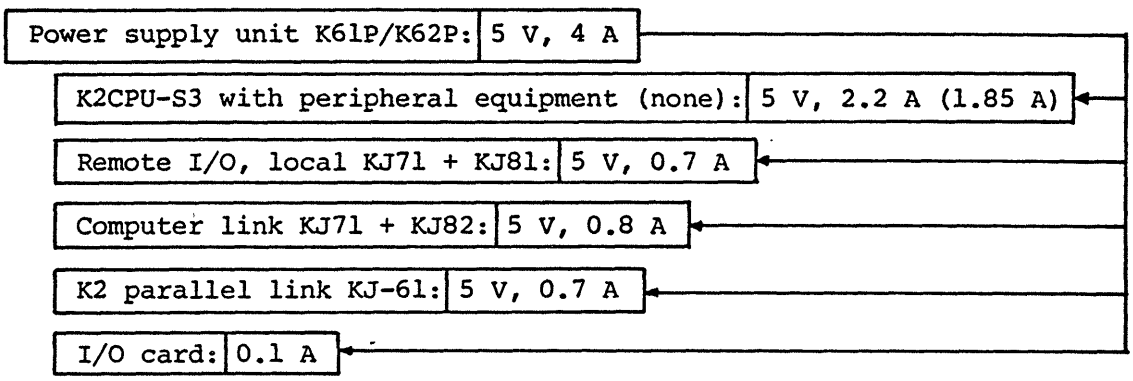
Note: Use of the same power supply for all controllers and simultaneous power ON also may be executed.

(2) Parallel off is executed automatically for a local station with trouble, and the master station detects the trouble station by means of the data register D124, but for restoration of the parallel off local station, the power supply for the master station must be switched off and on again or the master station must be reset with the reset switch.

9. Caution items for handling

9.1. Power supply capacity

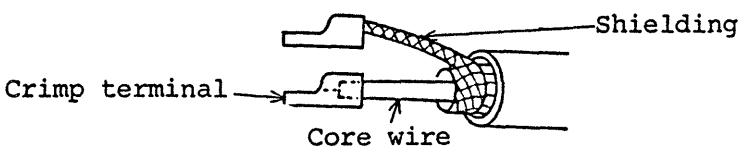
The power supply capacity of the power supply unit (K61P/K62P) and the 5 V load currents of the KJ71 and the I/O units are as follows.



When the above data link units are used installed in the basic base of the K2CPU, installation must be executed after calculation that the 5 V, 4 A of the power supply unit are not exceeded.

9.2. Coaxial cable termination method

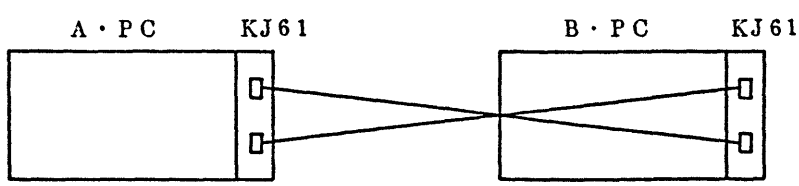
Apply crimp terminals as shown below and caulk them sufficiently.



Insert the shielding of the core wire into the crimp terminal and execute caulking.

9.3. Data link system processing time

9.3.1. Data link system 1 between K2CPUs



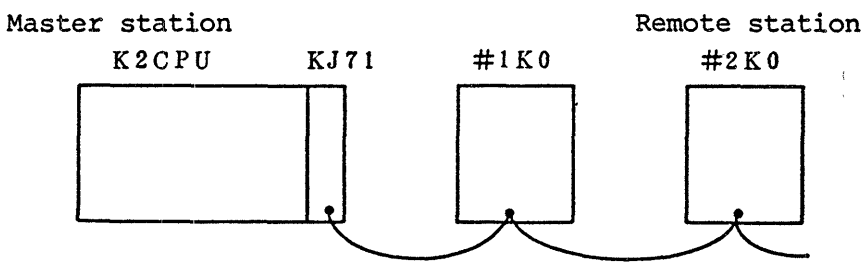
(1) Processing time

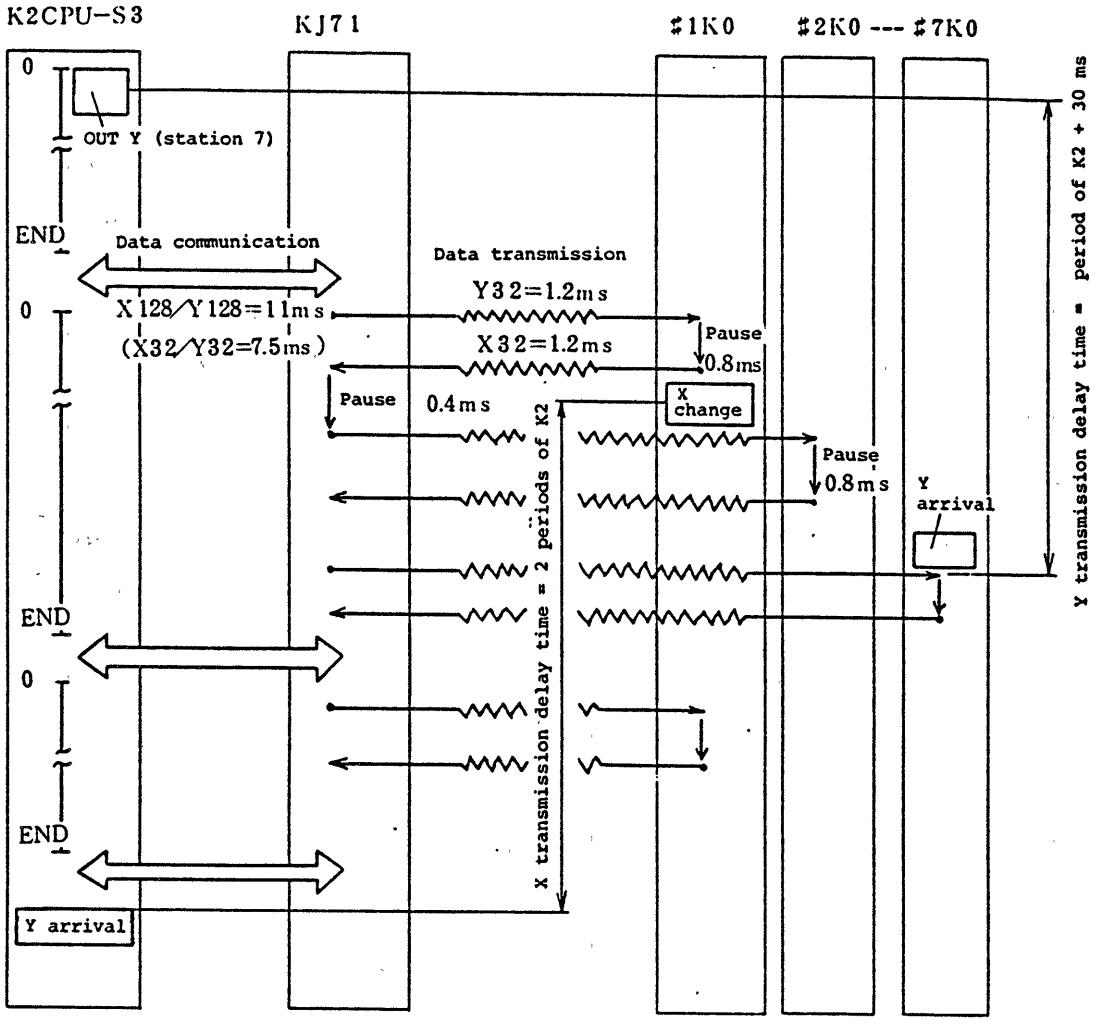
When a transmission request from the opposite side comes during 0 to END of the operation, reception will be executed.
After the END instruction, a transmission request is put out to the opposite side and transmission is executed.The time required for this transmission signal is 15 to 20 ms (per KJ61). Accordingly, the operation processing time is extended by 15 to 20 ms when one KJ61 is installed.
For a system with 3 units in parallel operation (Fig. 5.3), the processing operation time is extended by max. 30 to 40 ms when two KJ61 are installed for each unit.

(2) Propagation delay time

The A.PC output is transmitted to the opposite side B.PC after the END instruction. The opposite side executes reception unless data instructions are being executed. Accordingly, the A.PC output is transmitted to the opposite side with a delay of one period. The transmission from the opposite side also is transmitted with a delay of one period of the opposite side.

9.3.2. Remote I/O system with K2CPU and K0 unit of system 2





(1) Processing time

The operation repeats 0 to END. After END, the K2CPU executes data communication with the KJ71, and afterwards it gives the command for transmission and reception with the substation to the KJ71 and simultaneously again executes operation from 0 to END. Accordingly, the operation processing time is extended by the data communication time with the KJ71 (about 11 ms for X/Y = 256 points).

(2) Transmission delay time

The K2CPU is transmitted to the substation after the next END. Assuming that the output has changed near the step No. 0, the transmission delay time to station #7 becomes 1 period of the K2CPU + 30 ms.

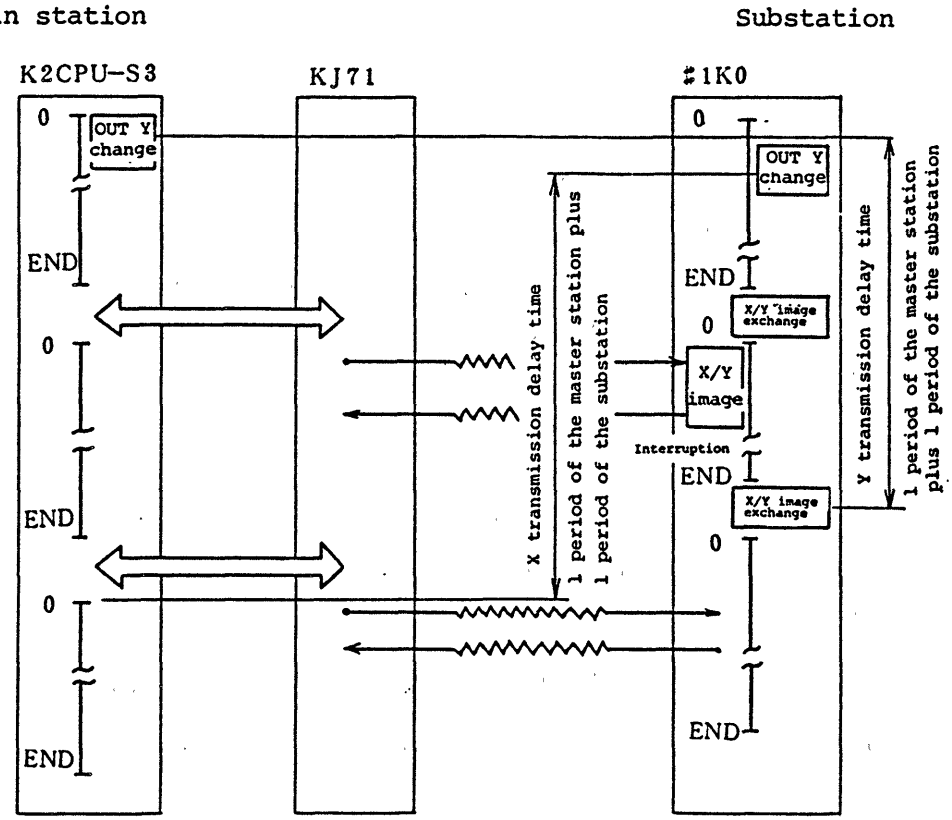
These 30 ms are the data communication time with the K2-KJ71 for 256 X/Y link points plus the transmission and reception time to the stations #1 to #7. Reversely, assuming that the input signal of the substation (station #1) has changed after the transmission and reception, the transmission time to the K2CPU is delayed in the worst case by 2 periods of the K2.

When the program step number of the K2CPU is extremely low, intermittent transmission and reception control is executed in the KJ71. As this control time is 20 ms, one period of the K2CPU is at least 20 ms.

9.3.3. Remote I/O system with K2CPU and K1/K2 I/O units of system 3

Processing speed and transmission delay are the same as for system 2.

9.3.4. Dispersed control system with K2CPU and K0 units of system 4



(1) Processing time

The operation repeats 0 to END. After END, the K2CPU executes data communication with the KJ71, and afterwards it gives the command for transmission and reception with the substation to the KJ71 and simultaneously again executes operation from 0 to END (transmission and reception and sequence operation are executed in parallel). Accordingly, the operation processing time is extended by the data communication time with the KJ71 (about 11 ms for X/Y = 256 points). The substation executes transmission and reception from the main station during operation from 0 to END. Accordingly, the operation processing time is extended just by the transmission and reception time (about 4 ms with X/Y = 64 points).

However, when the program step number (A) of the master station is low and the program step number (B) of the substation is high, the operation processing time is extended by B/A x about 4 ms. (Even when the program step number of the main station is low, intermittent control for transmission and reception is executed with 20 ms.)

(2) Transmission delay time

The K2CPU output is transmitted to the substation after the next END. Assuming that this output changes near the step number 0, the transmission delay to the substation becomes one period of the K2CPU.

Assuming that the substation has executed transmission and reception after END, then the transmission and reception contents are exchanged with the image memory used by the programmable controller at the next END, so that the delay time for transmission of the output of the main station to the substation is one period of the main station plus one period of the substation. The delay for output from the substation to the main station also is one period of the main station plus one period of the substation.

9.3.5. Dispersed control system with K2CPU and K2CPU of system 5

(1) Processing time

The main station operation repeats 0 to END. After END, the K2CPU executes data transmission to the KJ71, and afterwards it gives the command for transmission and reception with the substation to the KJ71 and simultaneously again executes operation from 0 to END (transmission and reception and sequence operation are executed in parallel). Accordingly, the operation processing time is extended by the data communication time with the KJ71 (about 11 ms for X/Y = 256 points).

The substation operation also repeats 0 to END. After END, the K2CPU executes data communication with the KJ71. The required time for this data communication is 3.5 ms for X/Y = 64 points. Accordingly, the operation processing time is extended by 3.5 ms.

(2) Transmission delay time

The K2CPU output is transmitted to the substation after the next END. The substation executes exchange with the image memory used by the programmable controller after END. Assuming change near the program step number 0, the output of the main station will be transmitted with a delay of one period of the main station plus one period of the substation. Assuming change near the program step number 0, the output of the substation also will be transmitted with a delay of one period of the main station plus one period of the substation.

9.3.6. System 6, computer link

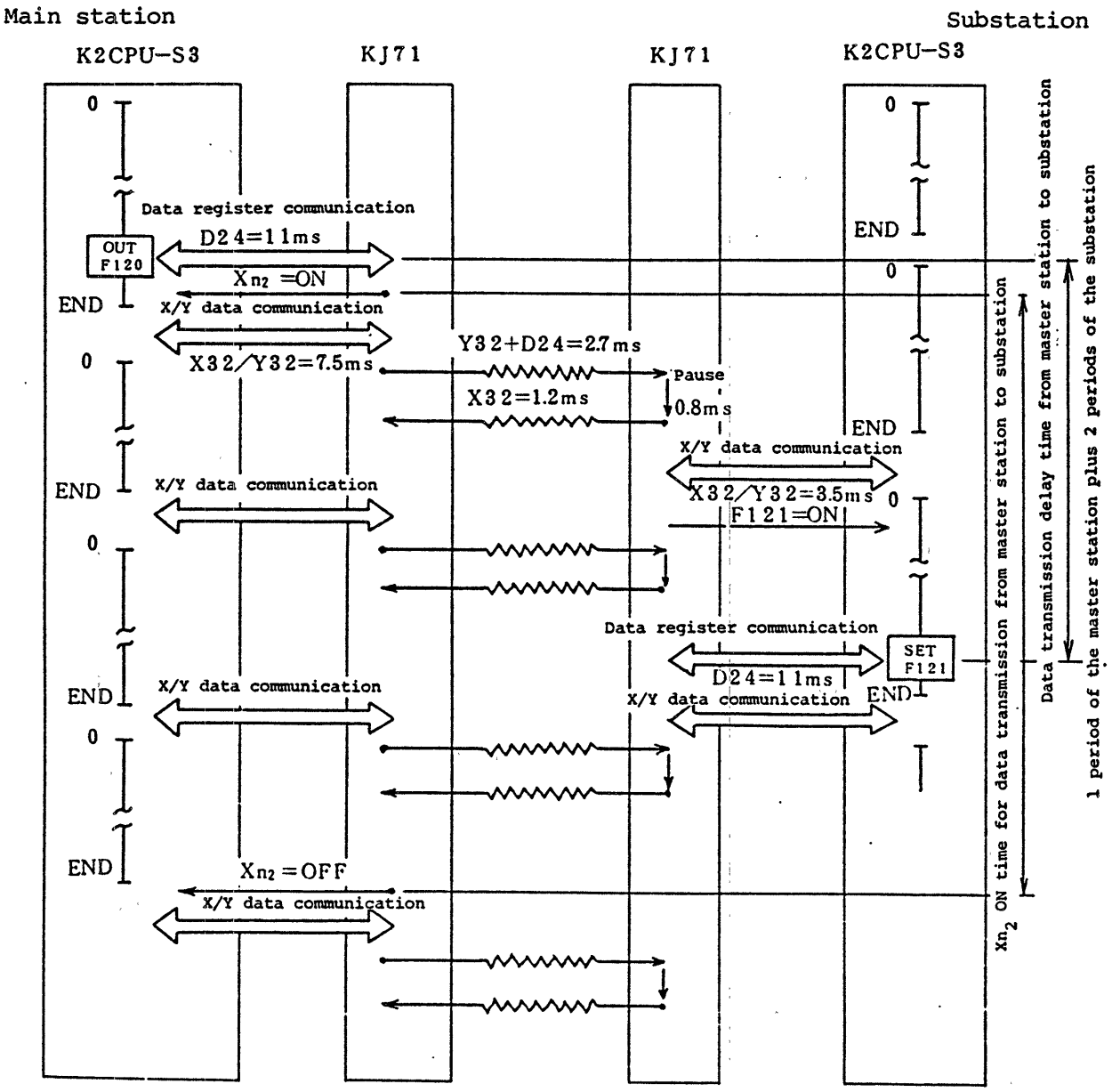
(1) Processing speed

When the computer link unit (KJ71 + KJ82 + L4ROM) is installed, response to access from the computer will be made during sequence instruction execution during processing of operation from 0 to END.
When there is no access, the operation processing time 0 to END) is extended by about 5%.
When there is access, the operation processing time will be extended by about 1 ms per byte.
The computer link applies access to the K2CPU at a rate of once every 10 ms.
Accordingly, the operation processing time (0 to END) with continuous access is extended by about 10%.

9.3.7. Data link with dispersed control

In addition to the X/Y link, a data register (D) link also is possible. As the delay time is longer than for the X/Y data link, caution is required for use.

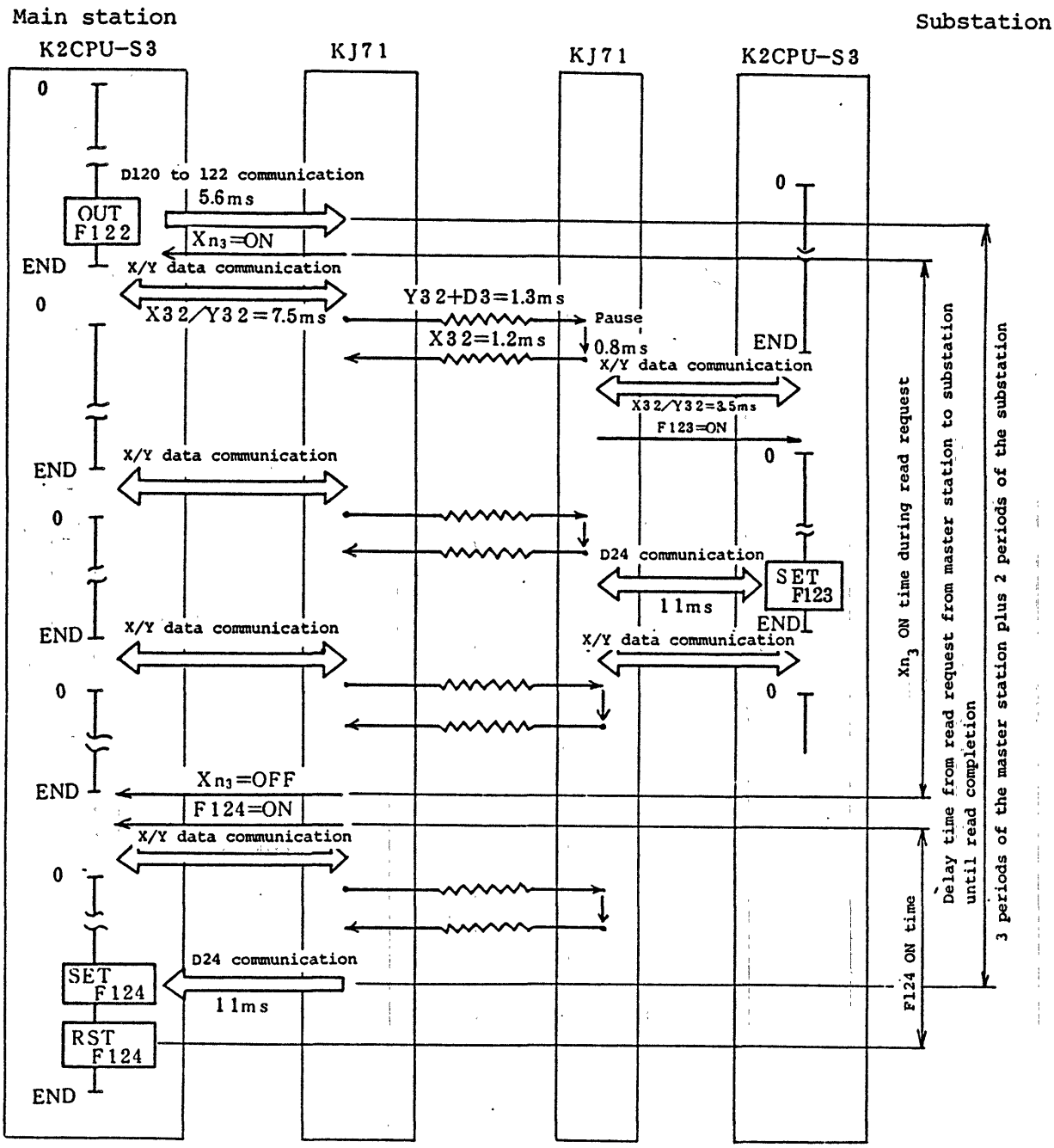
(1) Write request from main station to substation (F120)



The processing time is extended by about 11 ms for the data register max. simultaneous 24 points (D122 = 24).

The transmission delay time for a write request from the main station to the substation is one period of the main station plus one period of the substation. However, the ON time of Xn_2 during transmission is 2 periods of the main station plus 2 periods of the substation.

(2) Read request from the main station to the substation



The processing time is about 11 ms for the data register max. simultaneous 24 points (D122 = 24).
The transmission delay time for a read request from the main station to the substation is 3 periods of the main station plus 2 periods of the substation. The required time until read completion is the sum of the Xn_3 ON time during reception (2 periods of the main station plus 2 periods of the substation) and the F124 ON time of read completion (one period of the main station).

9.4. Scan time limitation

For the data link system, the scan time (operation processing time for one period) becomes longer, so that reference should be made to the technical note No. 44 (BCN-85023) and care should be taken.
The check time for the operation congestion detection time (WDT) of the programmable controller is 0.1 s. When resetting of WDT is executed after END instruction execution, the scan time becomes more than 0.1 s, a WDT error is caused, and the entire output becomes OFF from the hardware.

9.5. Instantaneous stop

The MELSEC-K series continues operation with instantaneous stop within 20 ms, but for this data link system, operation continuation is not possible with a short instantaneous stop. Accordingly, considerations should be made to prevent instantaneous stop of the power supply.

9.6. Power failure holding function

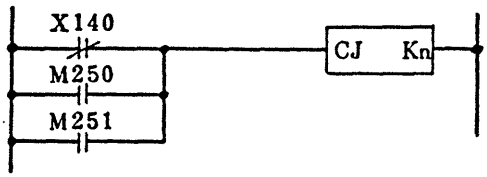
The power failure holding function also can be used for the data link system. However, the following considerations should be made for the program.

(1) On the side of the master programmable controller

Execute programming for X (Y output of the substation) data link data power failure holding so that the power failure holding program is bypassed by the CJ instruction when the transmission signals X100 and X180 of Fig. 5.12 are OFF.

(2) On the side of the local programmable controller

For X (Y output of the main station) data link data power failure holding, execute programming in the same way so that the program for power failure holding is bypassed by the CJ instruction for X140 of Fig. 5.14 and M250 and M251 as follows.



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IB(NA)64457-A(8503)R0D Printed in Japan